

Appendix D

Appendix D: QVGA Schematic

The QVGA Controller comprises two PC boards, designated the QED Board and the QVGA Board.

- ⇒ The QED Board contains the processor, RAM and Flash memory, digital I/O, A/D and D/A.*
- ⇒ The QVGA Board contains power conditioning,, display and touchscreen interface circuits, Wildcard module ports, and additional RAM and Flash memory.*
- ⇒ This Appendix provides complete circuit schematics for each board.*

QED Board Schematic

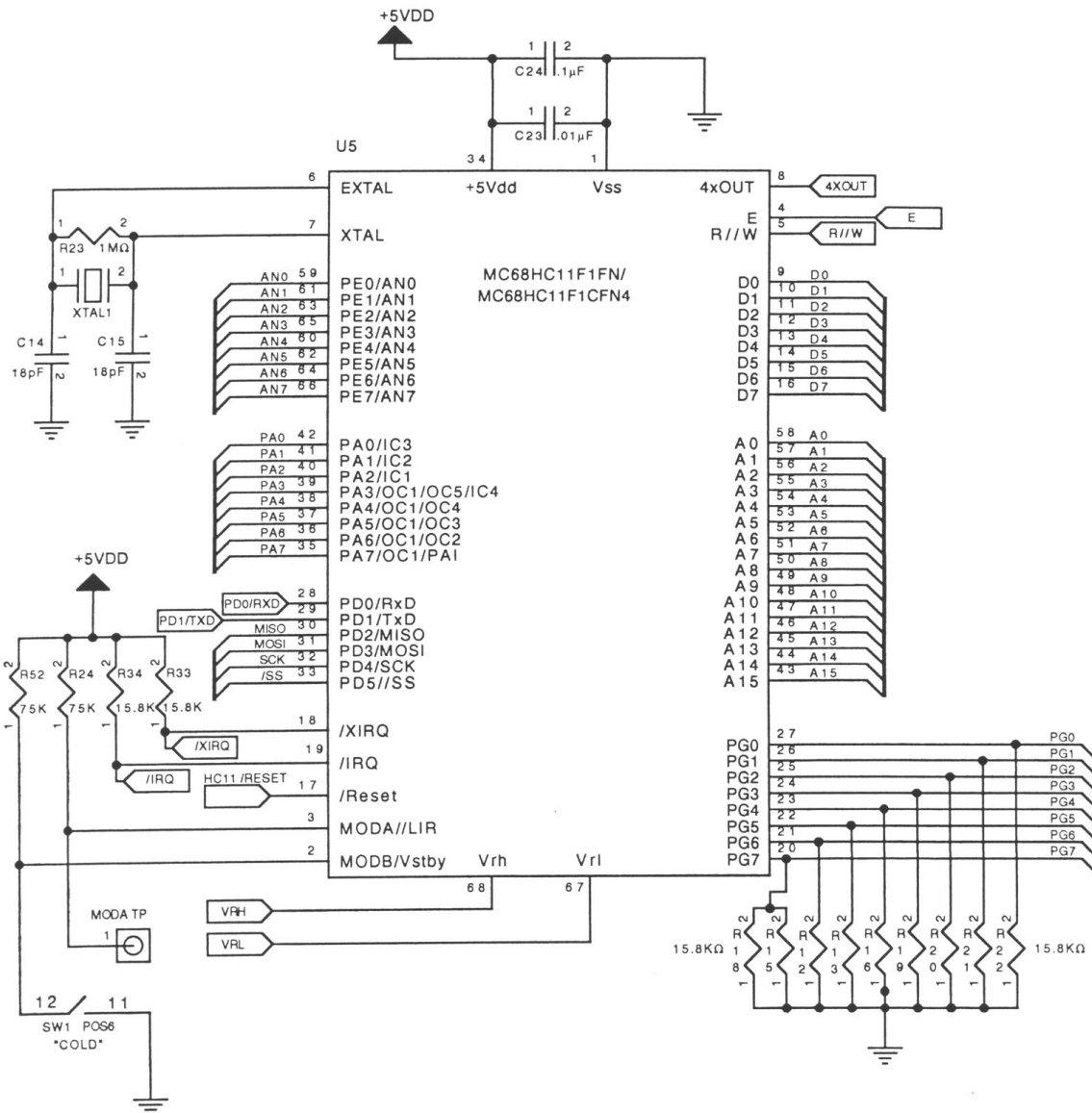


Figure D-1 QED Board (PN: QED-4-QVGA) Processor.



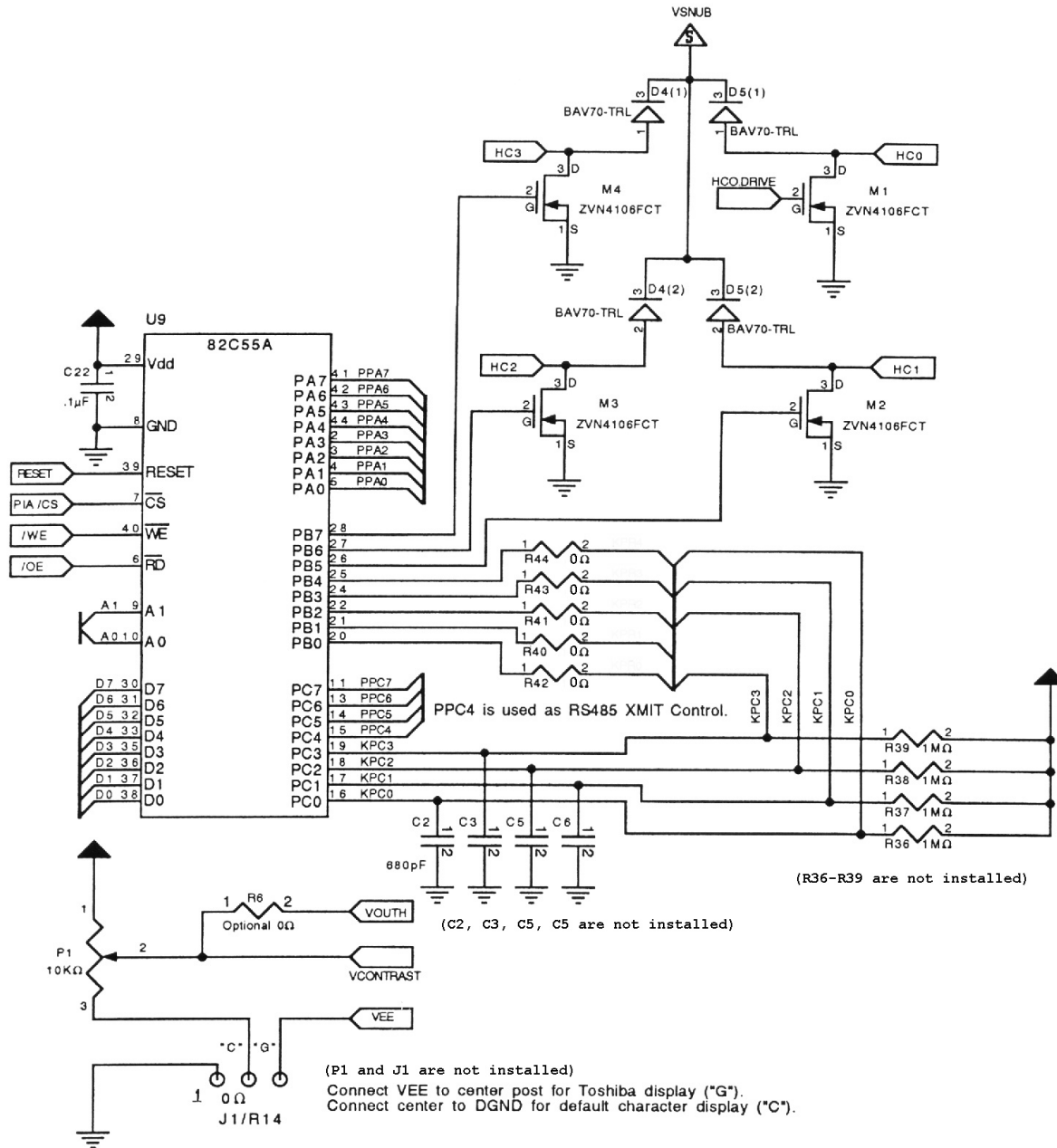


Figure D-3 QED Board PIA and High Current Drivers.

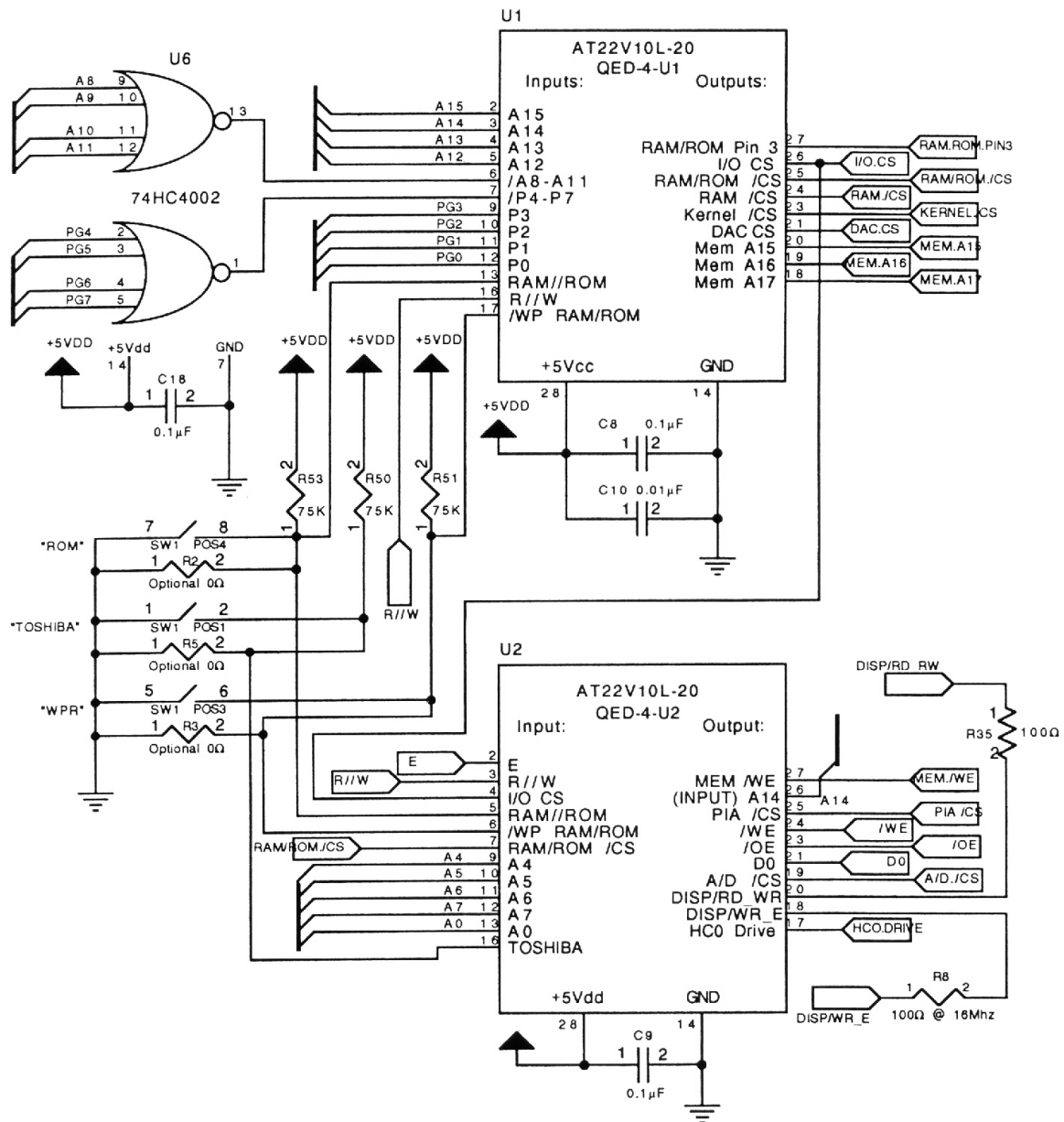


Figure D-4 QED Board PAL Glue Logic.

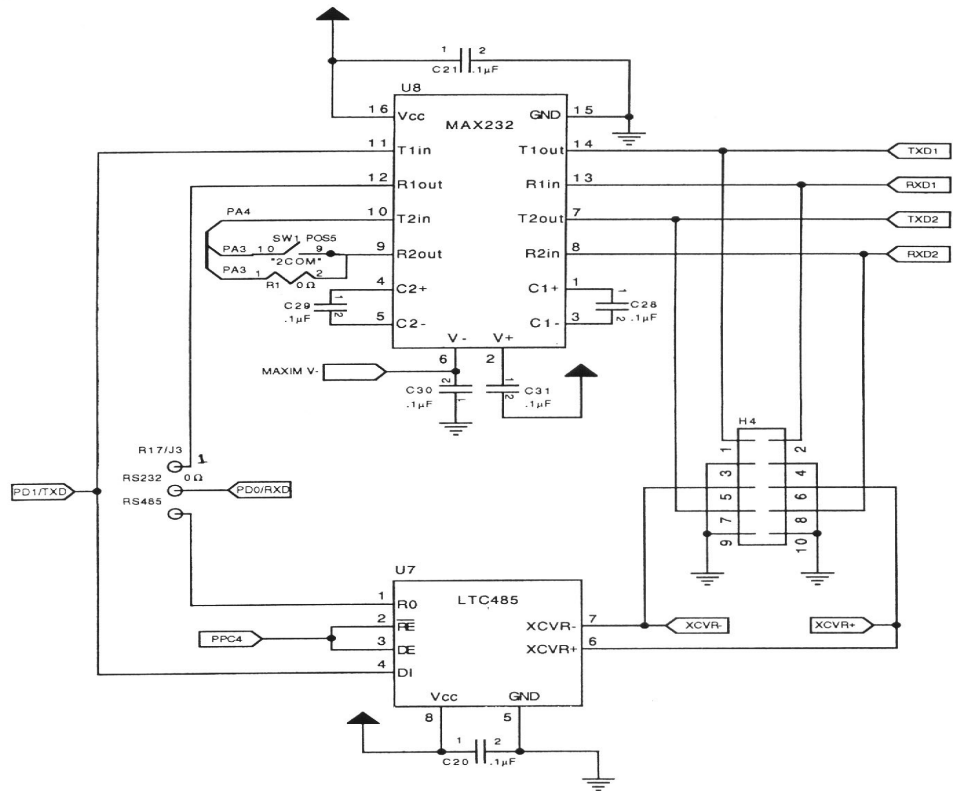


Figure D-5 QED Board Serial Communications Drivers.

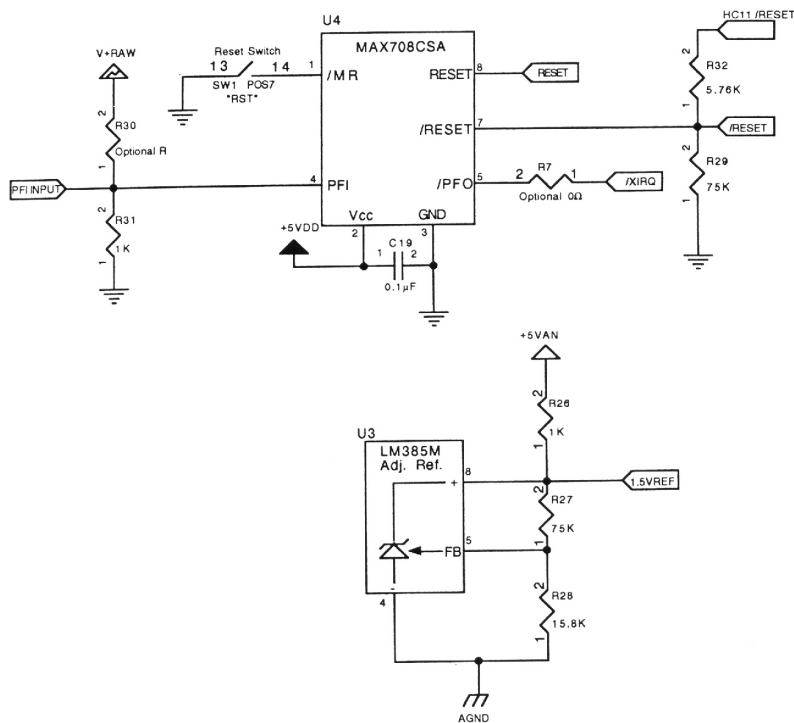


Figure D-6 QED Board Reset Circuitry.

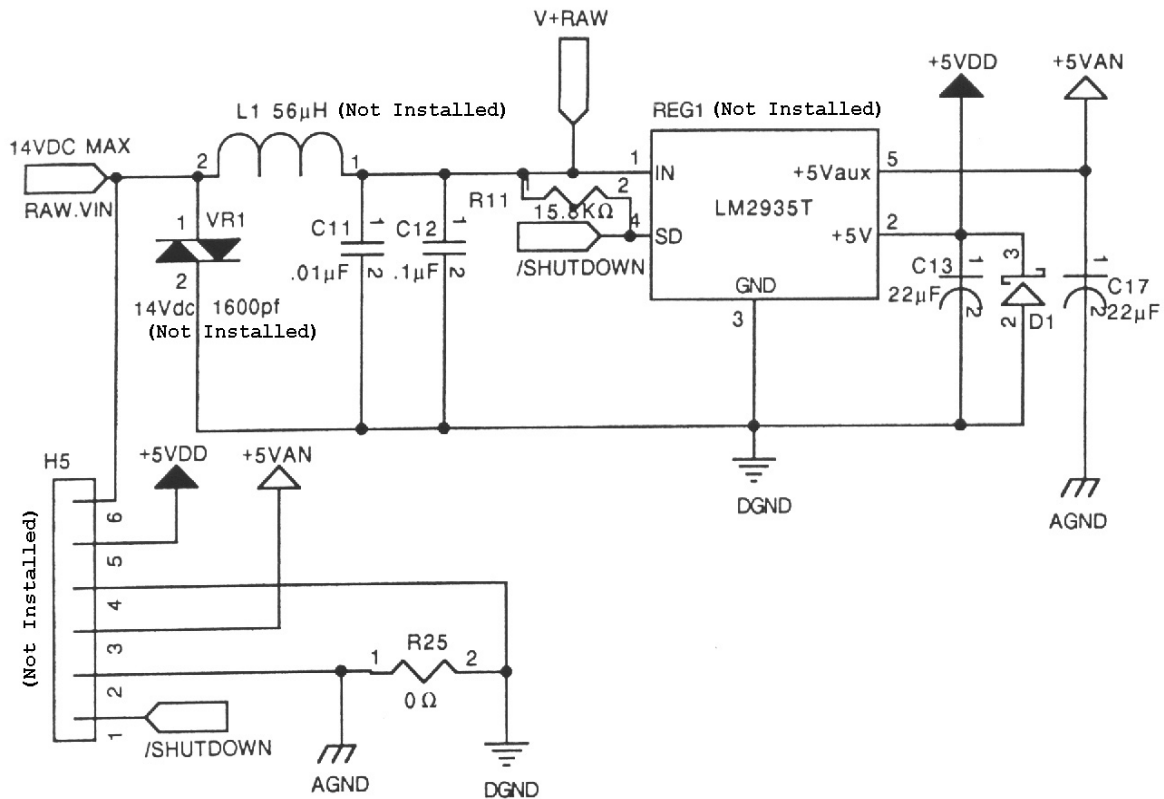


Figure D-7 QED Board Power Conditioning. (The regulator and input filter are not installed; the QED-4-QVGA Board receives filtered and regulated power from the QVGA Board).

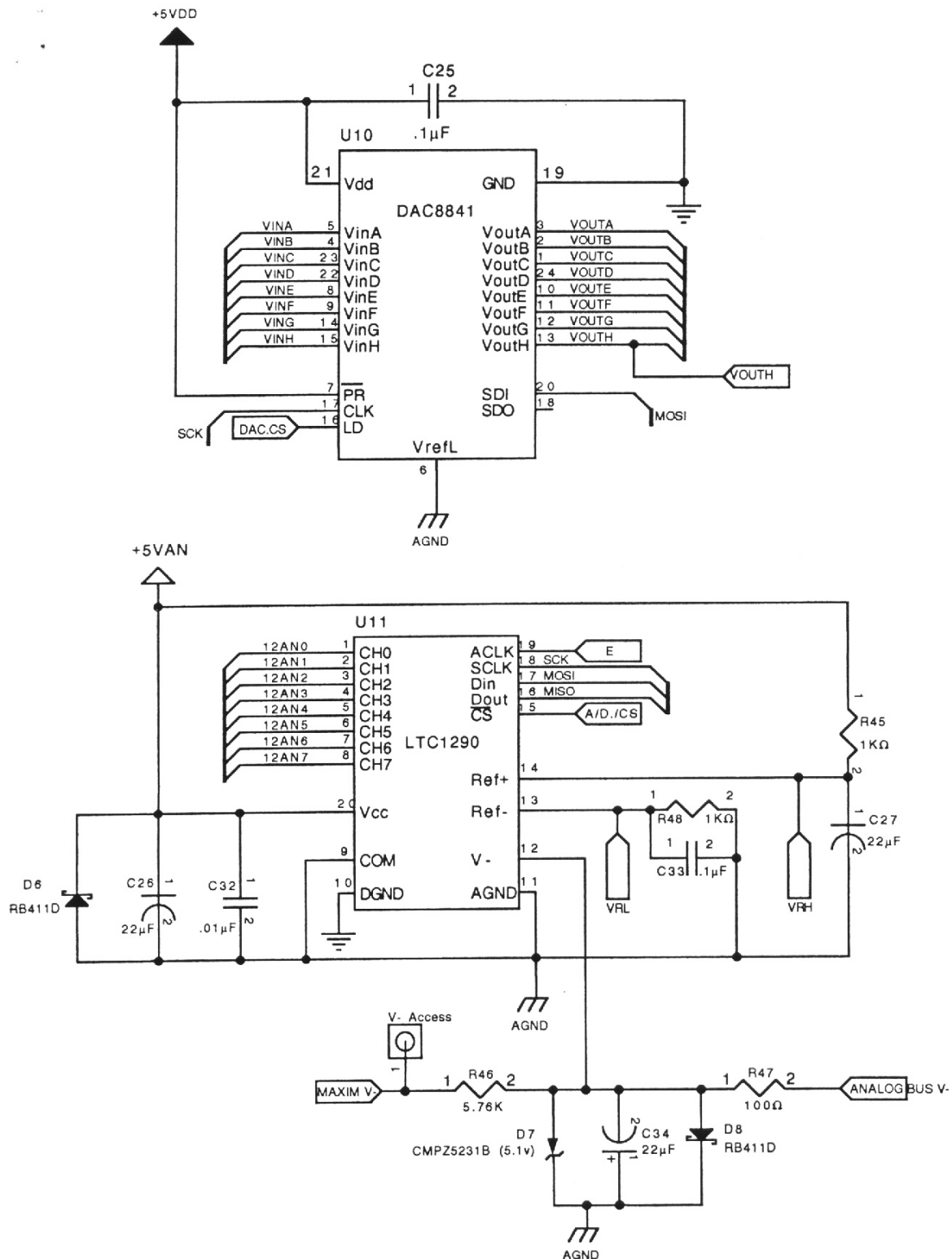


Figure D-8 QED Board 12-bit A/D and 8-bit DAC.

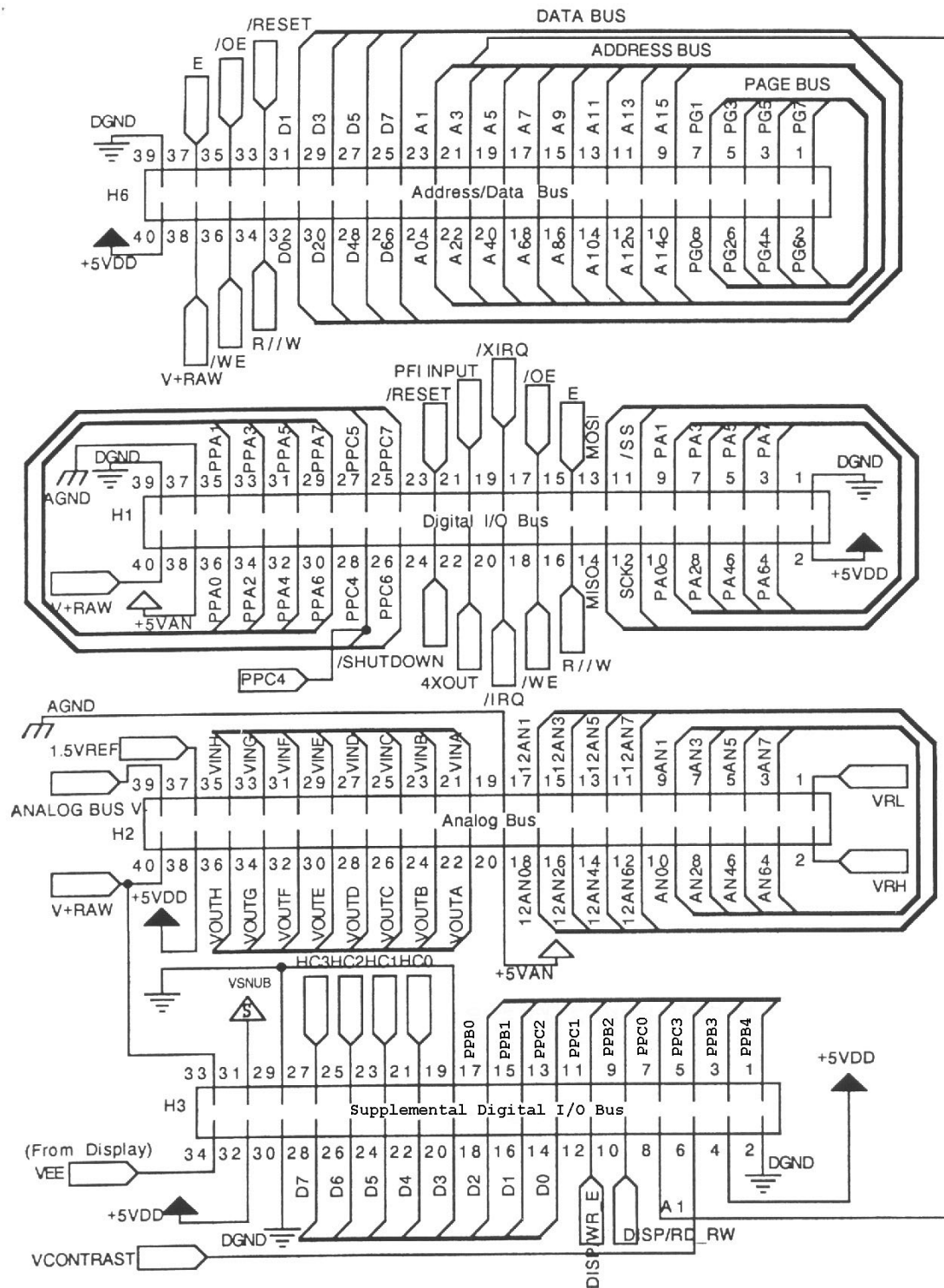


Figure D-9 QED Board Connector Pin-Outs.

QVGA Board Schematic

1	2	3	4	5	6
A	<div>QVGA_CPLD QVGA_CPLD.Sch</div> <div>Page 1</div> <div>R/W /MOD_OE /MOD_WE E DISPLAY_CS /RAM_CS /FLASH_CS /MOD_CS /MOD1_CS /BEEP_ON /RESET DIO_71 ADIO_71 PGIO_71 /PEN_DATA_AVAIL SCK PDS/SS MOSI TDO_MAIN TCK TMS TDO_DISPLAY /PEN_CS</div>				
	<div>memory memory.Sch</div> <div>Page 3</div> <div>/FLASH_CS /WE /OE /RAM_CS PGIO_71 AIO_151 DIO_71</div>				
B	<div>Display_Controller Display_Controller.Sch</div> <div>Page 2</div> <div>DIO_71 VDIO_81 PGIO_71 16MHZ /RESET FLM_VSYNC DATA_LOAD_HSYNC SHIFT_CLOCK CCFL_ON /DACPOT_CS /DACPOT_UP LCD_ON DISP_AIO_161 DRDY_ENAB DIO_151 TDO_MAIN TCK TMS TDO_DISPLAY DISPLAY_CS AIO_151 R/W E AIO_151 DISPLAY_CS</div>				
	<div>LCD_Bias LCD_Bias.Sch</div> <div>Page 5</div> <div>/DACPOT_CS /DACPOT_UP COLOR_VCON /DACPOT_CS /DACPOT_UP MONO_VCON V-BIAS MONO_VEE /SHDN V-RAW LCD_ON /BEEP_ON EXT_VIN SWITCHED_VIN</div>				
C	<div>Touch_CCFI Touch_CCFI.Sch</div> <div>Page 4</div> <div>/TOUCH_X+ /TOUCH_Y+ /TOUCH_X- /TOUCH_Y- /PEN_DATA_AVAIL SCK MOSI /PEN_CS MISO CCFL_ON +12V/+5V_ALT</div>				
	<div>QED_Middle_Headers QED_Middle_Headers.Sch</div> <div>Page 8</div> <div>AIO_151 V-RAW DIO_71 /OE ADIO_71 /RESET PGIO_71 E MOSI MISO /SVAN SCK R/W PDS/SS V-RAW MISO</div>				
D	<div>Touchscreen_Headers Touchscreen_Headers.Sch</div> <div>Page 7</div> <div>VDIO_81 +12V/+5V_ALT COLOR_VCON MONO_VEE MONO_VCON TOUCH_Y+ TOUCH_X- TOUCH_Y- TOUCH_X+ FLM_VSYNC DATA_LOAD_HSYNC SHIFT_CLOCK /SHDN DRDY_ENAB</div>				
	<div>power power.Sch</div> <div>Page 6</div> <div>V-RAW +12V/+5V_ALT /SHDN +SVAN V-RAW EXT_VIN SWITCHED_VIN</div>				
A	<div>QVGA_Controller_Board QVGA_Controller_Board.Sch</div> <div>Page 1</div> <div>VDIO_81 PGIO_71 16MHZ /RESET FLM_VSYNC DATA_LOAD_HSYNC SHIFT_CLOCK CCFL_ON /DACPOT_CS /DACPOT_UP LCD_ON DISP_AIO_161 DRDY_ENAB DIO_151 TDO_MAIN TCK TMS TDO_DISPLAY DISPLAY_CS AIO_151 R/W E AIO_151 DISPLAY_CS</div>				
	<div>QED_Middle_Headers QED_Middle_Headers.Sch</div> <div>Page 8</div> <div>AIO_151 V-RAW DIO_71 /OE ADIO_71 /RESET PGIO_71 E MOSI MISO /SVAN SCK R/W PDS/SS V-RAW MISO</div>				
B	<div>LCD_Bias LCD_Bias.Sch</div> <div>Page 5</div> <div>/DACPOT_CS /DACPOT_UP COLOR_VCON /DACPOT_CS /DACPOT_UP MONO_VCON V-BIAS MONO_VEE /SHDN V-RAW LCD_ON /BEEP_ON EXT_VIN SWITCHED_VIN</div>				
	<div>power power.Sch</div> <div>Page 6</div> <div>V-RAW +12V/+5V_ALT /SHDN +SVAN V-RAW EXT_VIN SWITCHED_VIN</div>				
C	<div>Touch_CCFI Touch_CCFI.Sch</div> <div>Page 4</div> <div>/TOUCH_X+ /TOUCH_Y+ /TOUCH_X- /TOUCH_Y- /PEN_DATA_AVAIL SCK MOSI /PEN_CS MISO CCFL_ON +12V/+5V_ALT</div>				
	<div>QED_Middle_Headers QED_Middle_Headers.Sch</div> <div>Page 8</div> <div>AIO_151 V-RAW DIO_71 /OE ADIO_71 /RESET PGIO_71 E MOSI MISO /SVAN SCK R/W PDS/SS V-RAW MISO</div>				
D	<div>Touchscreen_Headers Touchscreen_Headers.Sch</div> <div>Page 7</div> <div>VDIO_81 +12V/+5V_ALT COLOR_VCON MONO_VEE MONO_VCON TOUCH_Y+ TOUCH_X- TOUCH_Y- TOUCH_X+ FLM_VSYNC DATA_LOAD_HSYNC SHIFT_CLOCK /SHDN DRDY_ENAB</div>				
	<div>power power.Sch</div> <div>Page 6</div> <div>V-RAW +12V/+5V_ALT /SHDN +SVAN V-RAW EXT_VIN SWITCHED_VIN</div>				

Figure D-10 QVGA Board Schematic Signal Directory.



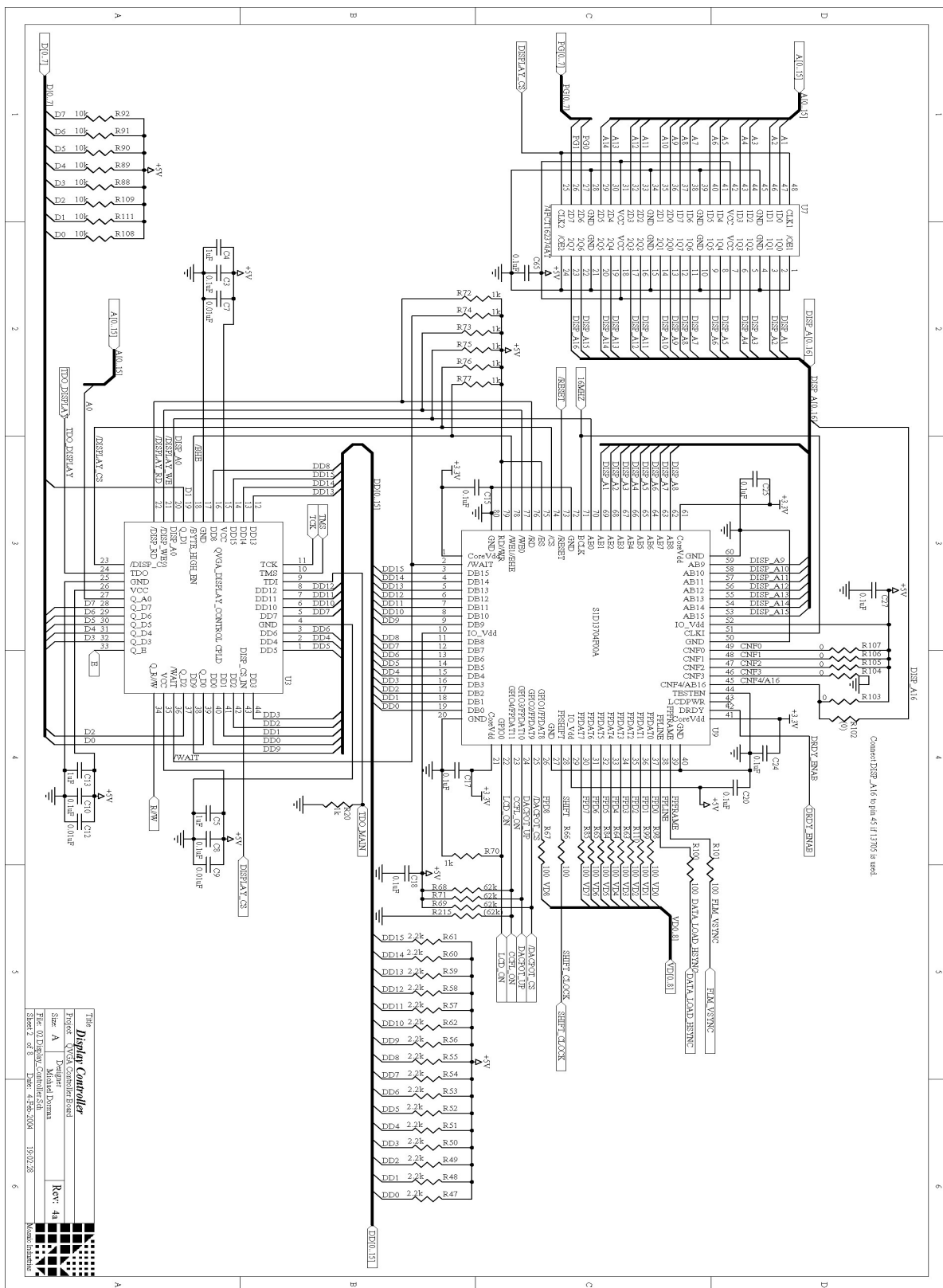


Figure D-12 QVGA Board Display Controller.

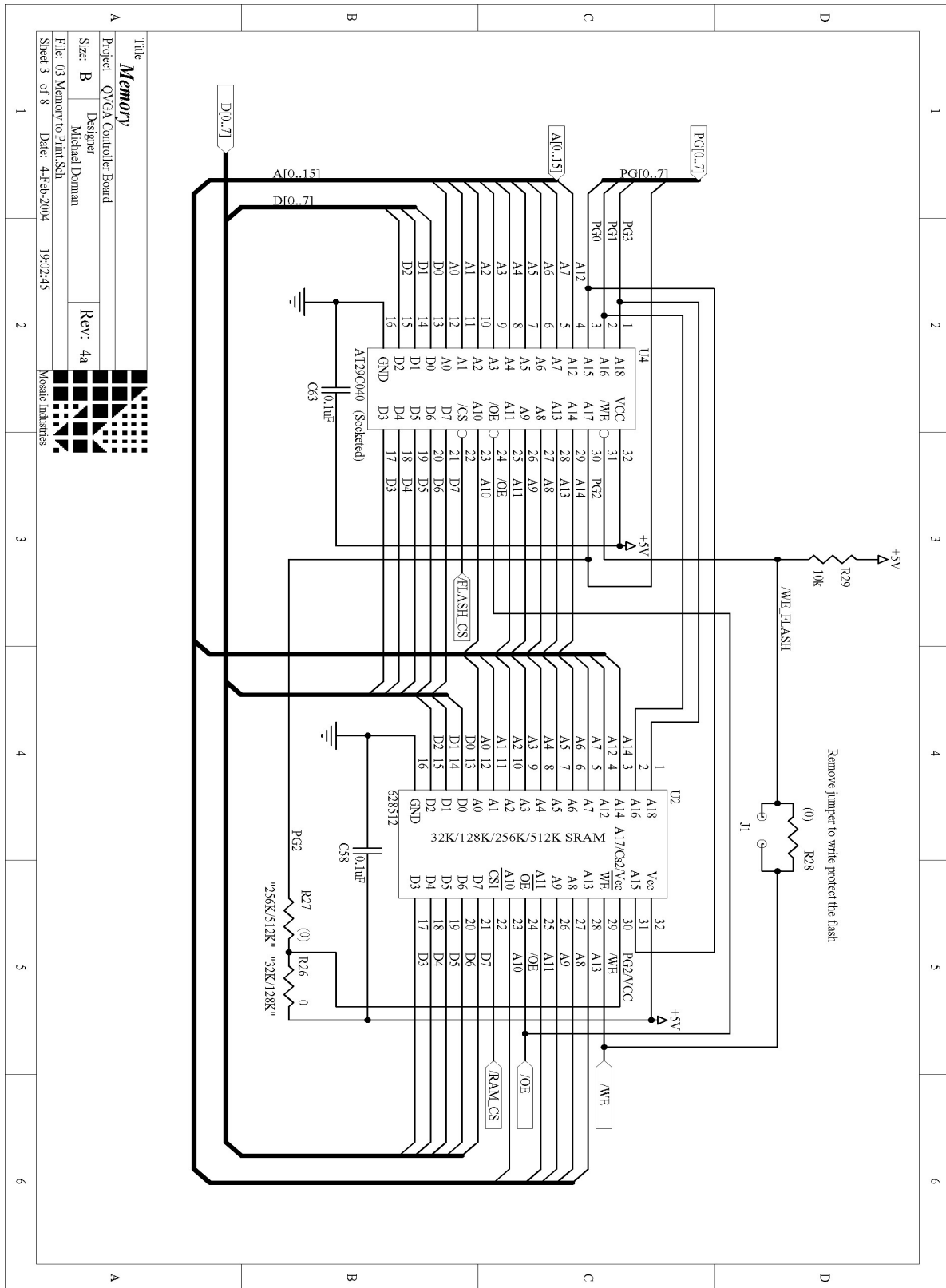
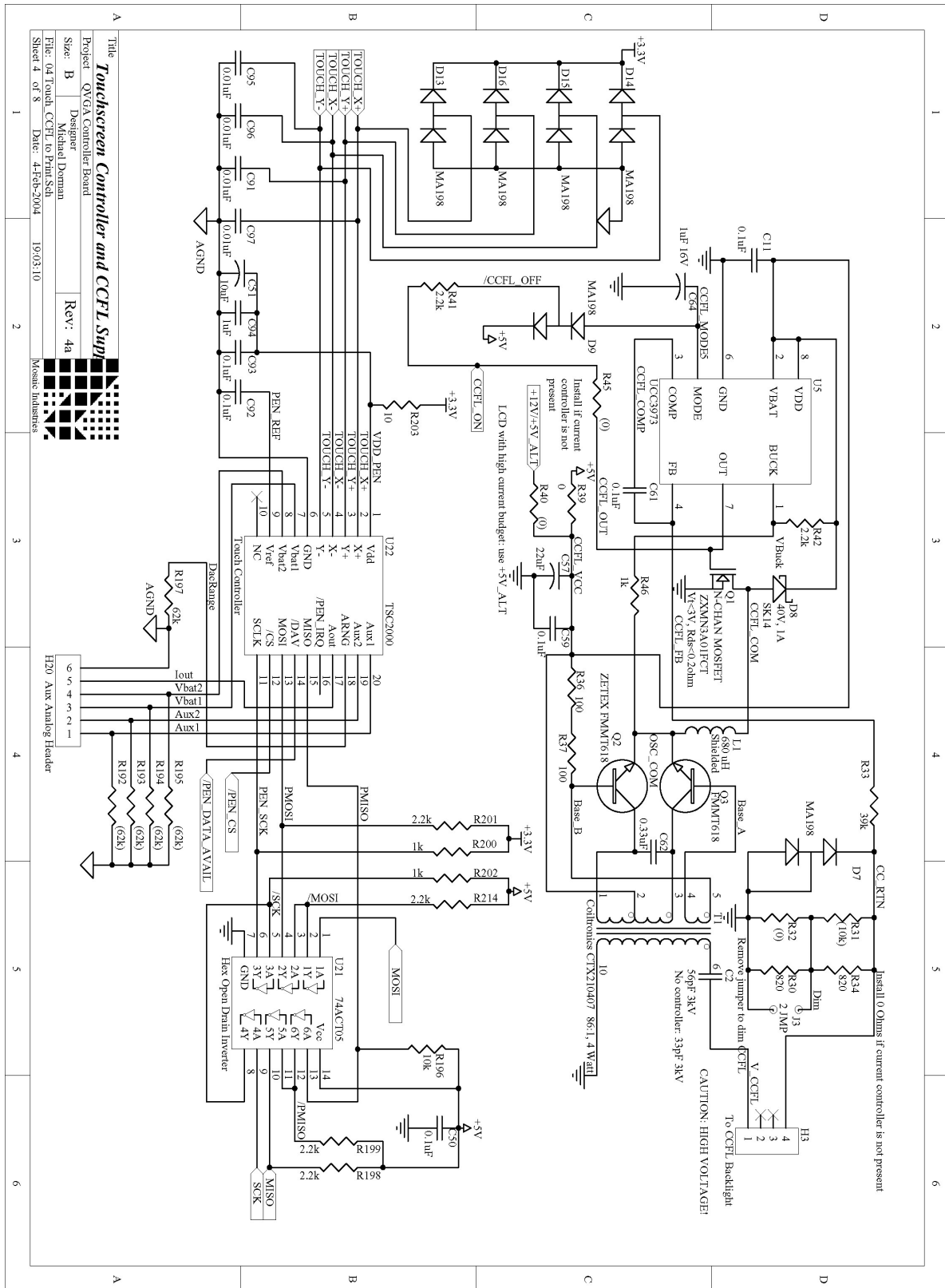
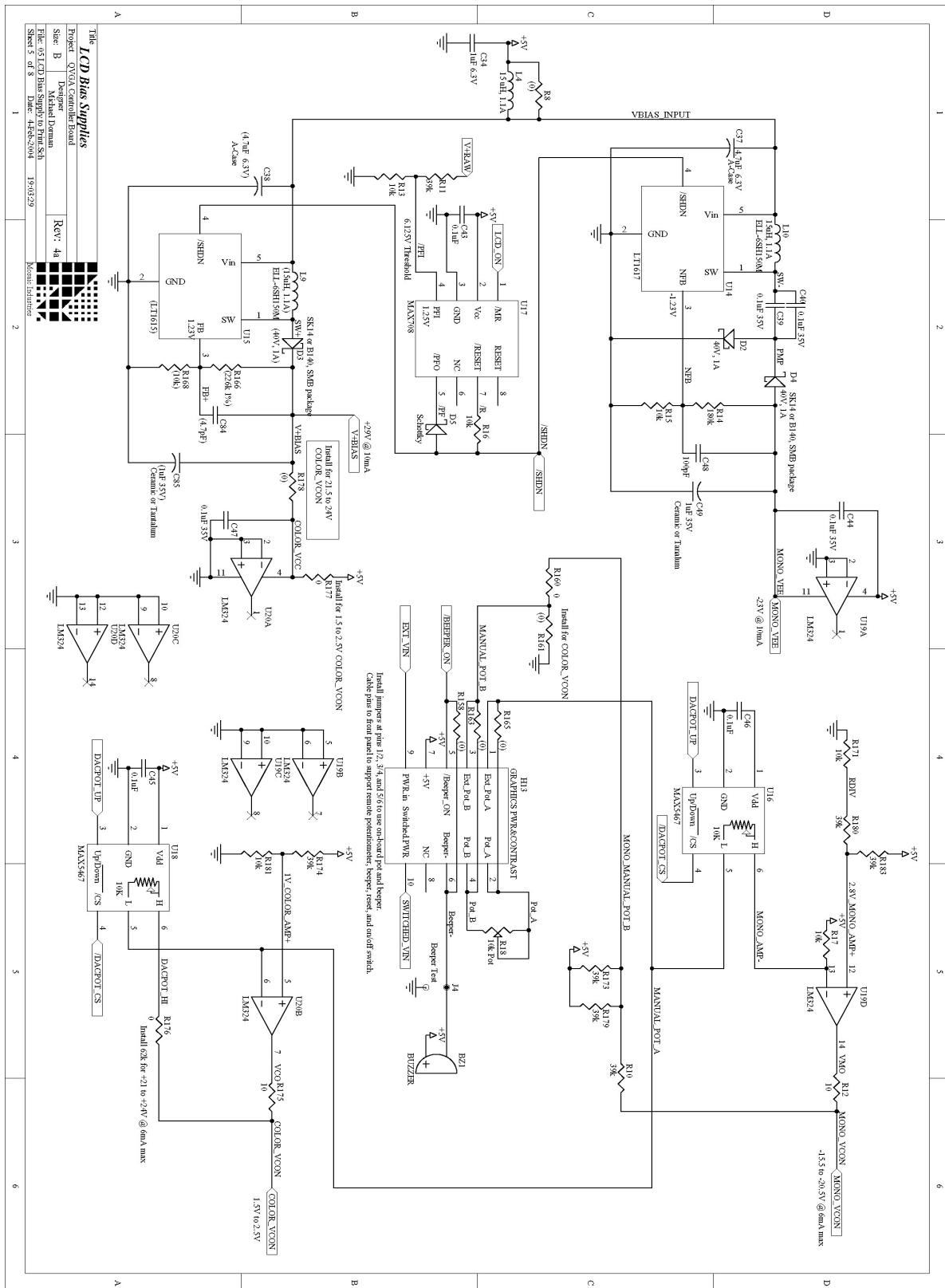


Figure D-13 QVGA Board Memory.





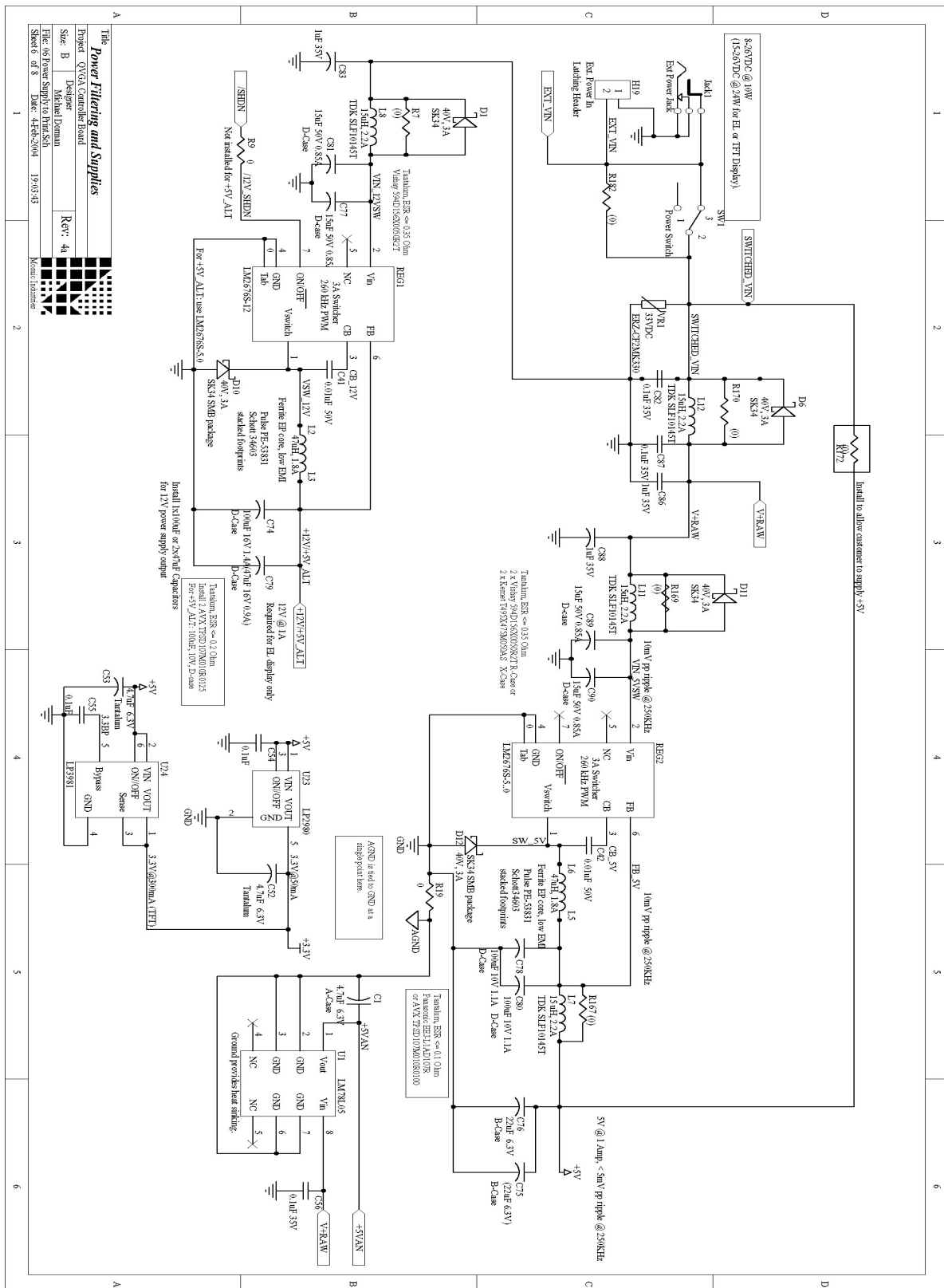


Figure D-16 QVGA Board Power.

