ECT_16B8C
Block User Guide
V02.03

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Motorola Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
0.1	2-Sep-99	2-Sep-99		Original draft. Distributed only within Motorola QS9000 Verified.
0.2	24-Sep-99	24-Sep-99		• Changed the specs as per MSRS format. • Modified ECT16b8c Block diagram. • Modified IP Bus signal names and their description. • Modified ECT output signal names. • Deleted bits 3-0 of TSCR1 register in Register Map(Sheet 1 of 2). • Modified register addresses in the description of TSFRZ,WAIT,NORMAL mode(Modes of Operation). • In Figure 1-6 changed text font to Halvetica. • Renamed TMSK1 and TMSK2 register as TIE and TSCR2 also renamed TSCR as TSCR1. • Modified TFLG2 bit setting sentence. • Added explanation about the abbreviation(M clock,PACLK) used. • Removed duplication of lines at the end of register description of PACN3/PACN2. • Corrected the reset value of MCCNT from $FF to $FFFF in the description of register MCCTL. • Corrected Table format for delay counter select and Modulus counter Prescalar Select. • Corrected all the cross-references used in section 3 of the document. • Deleted and added some module specific signals. • Changed all interrupts from active LOW to active HIGH. • Added description about successful output comapre and forced output compare taking place simultaneously and their effect on flag. • Added abbreviation section. • In Fig 1-3 changed host data bus to IPbus.
0.3	25-Oct-99	25-Oct-99		• Changed block name in Section 2. • Removed signals ipp_ect_ic_ibe and ipp_ect_ic_offval from port list.
0.4	11-Nov-99	11-Nov-99		• Removed signal ipb_read & ipb_write from portlist. ipb_rwb added

Version Number	Revision Date	Effective Date	Author	Description of Changes
0.5	1-Dec-99	1-Dec-99		• Incorporated feedback received from Joachim Kruecken on 30-Nov-99
01.00	10-May-01	11-May-01		• formal changes for SRS compliance (cover, master pages, paragraph formats, register templates) • updated cross-references • marked TIMTST register description with ’non_cust’ tag
01.01	19-July-01			• Document names have been added • Names and Variable definitions have been hidden
01.02	10-Jan-02	10-Jan-02		• Note added in Section 3.3.18 for PACN1/PACN0
01.03	18-Jul-02	18-Jul-02		• Changed the register bit information of MCCTL on bits • ICLAT and FLMC
01.04	11-Nov-02	11-Nov-02		• Eliminated all references of "n" to "x" .e.g. IOSn to IOSx
02.00	24-Jun-03	24-Jun-03		• Functional change (Modifed TSCR1, DLYCT, MCCTL and introduced PTPSR, PTMCPSR registers) • •
02.01	10-Nov-03	18-Nov-03		•
02.02	05-Jul-04	05-Jul-04		• Included delay counter operational description in section 4.2.1.3 and updated version on cover sheet
02.03	12-Aug-04	12-Aug-04		• Included OC initialization description in section 4.2.2 and updated version on cover sheet.

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Section 1 Introduction

1.1 Overview

The HCS12 Enhanced Capture Timer module has the features of the HCS12 Standard Timer module enhanced by additional features in order to enlarge the field of applications, in particular for automotive ABS applications.

This design specification describes the standard timer as well as the additional features.

The basic timer consists of a 16-bit, software-programmable counter driven by a prescaler. This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from microseconds to many seconds.

A full access for the counter registers or the input capture/output compare registers will take place in one clock cycle. Accessing high byte and low byte separately for all of these registers will not yield the same result as accessing them in one word.

1.2 Features

- 16-Bit Buffer Register for four Input Capture (IC) channels.
- Four 8-Bit Pulse Accumulators with 8-bit buffer registers associated with the four buffered IC channels. Configurable also as two 16-Bit Pulse Accumulators.
- 16-Bit Modulus Down-Counter with 8-bit Prescaler.
- Four user selectable Delay Counters for input noise immunity increase.

1.3 Modes of Operation

STOP: Timer and modulus counter are off since clocks are stopped.

FREEZE: Timer and modulus counter keep on running, unless the TSFRZ bit in the TSCR1 register is set to one.

WAIT: Counters keep on running, unless the TSWAI bit in the TSCR1 register is set to one.

NORMAL: Timer and modulus counter keep on running, unless the TEN bit in the TSCR1 register or the MCEN bit in the MCCTL register are cleared.

1.4 Block Diagram

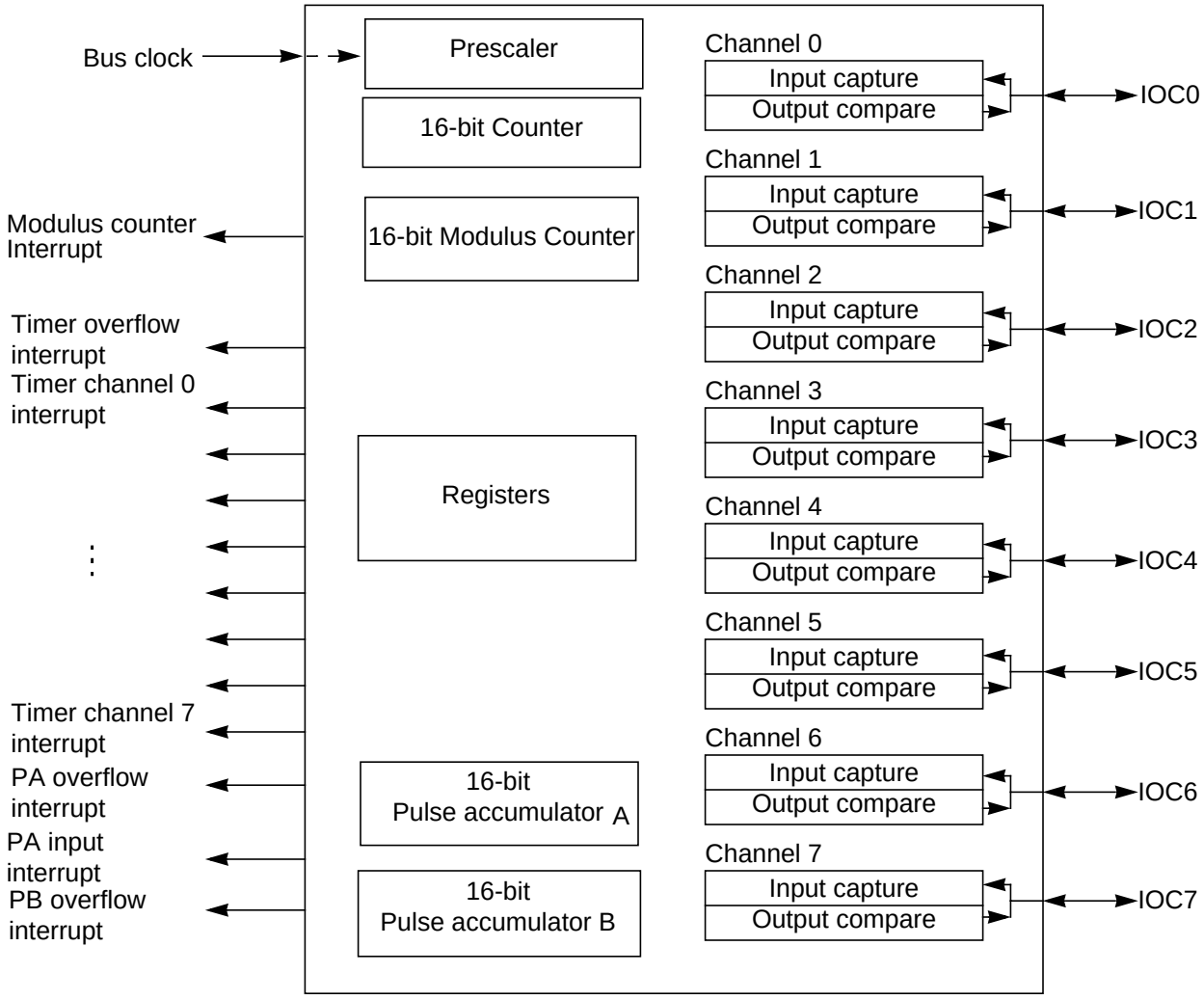


Figure 1-1 Timer Block Diagram

Section 2 Signal Description

2.1 Overview

The ECT_16B8C module has a total of 8 external pins.

2.2 Detailed Signal Descriptions

2.2.1 IOC7 - Input capture and Output compare channel 7

This pin serves as input capture or output compare for channel 7.

2.2.2 IOC6 - Input capture and Output compare channel 6

This pin serves as input capture or output compare for channel 6.

2.2.3 IOC5 - Input capture and Output compare channel 5

This pin serves as input capture or output compare for channel 5.

2.2.4 IOC4 - Input capture and Output compare channel 4

This pin serves as input capture or output compare for channel 4.

2.2.5 IOC3 - Input capture and Output compare channel 3

This pin serves as input capture or output compare for channel 3.

2.2.6 IOC2 - Input capture and Output compare channel 2

This pin serves as input capture or output compare for channel 2.

2.2.7 IOC1 - Input capture and Output compare channel 1

This pin serves as input capture or output compare for channel 1.

2.2.8 IOC0 - Input capture and Output compare channel 0

This pin serves as input capture or output compare for channel 0.

NOTE: *For the description of interrupts see Section 6 Interrupts.*

Section 3 Memory Map and Registers

3.1 Overview

This section provides a detailed description of all memory and registers.

3.2 Module Memory Map

The memory map for the ECT module is given below in **Table 3-1**. The Address listed for each register is the address offset. The total address for each register is the sum of the base address for the ECT module and the address offset for each register.

Table 3-1 Module Memory Map

Offset	Use	Access
$_00	Timer Input Capture/Output Compare Select (TIOS)	Read/Write
$_01	Timer Compare Force Register (CFORC)	Read/Write[1]
$_02	Output Compare 7 Mask Register (OC7M)	Read/Write
$_03	Output Compare 7 Data Register (OC7D)	Read/Write
$_04	Timer Count Register High (TCNT)	Read/Write[2]
$_05	Timer Count Register Low (TCNT)	Read/Write[2]
$_06	Timer System Control Register1 (TSCR1)	Read/Write
$_07	Timer Toggle Overflow Register (TTOV)	Read/Write
$_08	Timer Control Register1 (TCTL1)	Read/Write
$_09	Timer Control Register2 (TCTL2)	Read/Write
$_0A	Timer Control Register3 (TCTL3)	Read/Write
$_0B	Timer Control Register4 (TCTL4)	Read/Write
$_0C	Timer Interrupt Enable Register (TIE)	Read/Write
$_0D	Timer System Control Register2 (TSCR2)	Read/Write
$_0E	Main Timer Interrupt Flag1 (TFLG1)	Read/Write
$_0F	Main Timer Interrupt Flag2 (TFLG2)	Read/Write
$_10	Timer Input Capture/Output Compare Register0 High (TC0)	Read/Write[3]
$_11	Timer Input Capture/Output Compare Register0 Low (TC0)	Read/Write[3]
$_12	Timer Input Capture/Output Compare Register1 High (TC1)	Read/Write[3]
$_13	Timer Input Capture/Output Compare Register1 Low (TC1)	Read/Write[3]
$_14	Timer Input Capture/Output Compare Register2 High (TC2)	Read/Write[3]
$_15	Timer Input Capture/Output Compare Register2 Low (TC2)	Read/Write[3]
$_16	Timer Input Capture/Output Compare Register3 High (TC3)	Read/Write[3]

Table 3-1 Module Memory Map

$_17	Timer Input Capture/Output Compare Register3 Low (TC3)	Read/Write[3]
$_18	Timer Input Capture/Output Compare Register4 High (TC4)	Read/Write[3]
$_19	Timer Input Capture/Output Compare Register4 Low (TC4)	Read/Write[3]
$_1A	Timer Input Capture/Output Compare Register5 High (TC5)	Read/Write[3]
$_1B	Timer Input Capture/Output Compare Register5 Low (TC5)	Read/Write[3]
$_1C	Timer Input Capture/Output Compare Register6 High (TC6)	Read/Write[3]
$_1D	Timer Input Capture/Output Compare Register6 Low (TC6)	Read/Write[3]
$_1E	Timer Input Capture/Output Compare Register7 High (TC7)	Read/Write[3]
$_1F	Timer Input Capture/Output Compare Register7 Low (TC7)	Read/Write[3]
$_20	16-Bit Pulse Accumulator A Control Register (PACTL)	Read/Write
$_21	Pulse Accumulator A Flag Register (PAFLG)	Read/Write
$_22	Pulse Accumulator Count Register3 (PACN3)	Read/Write
$_23	Pulse Accumulator Count Register2 (PACN2)	Read/Write
$_24	Pulse Accumulator Count Register1 (PACN1)	Read/Write
$_25	Pulse Accumulator Count Register0 (PACN0)	Read/Write
$_26	16-Bit Modulus Down Counter Register (MCCTL)	Read/Write
$_27	16-Bit Modulus Down Counter Flag Register (MCFLG)	Read/Write
$_28	Input Control Pulse Accumulator Register (ICPAR)	Read/Write
$_29	Delay Counter Control Register (DLYCT)	Read/Write
$_2A	Input Control Overwrite Register (ICOVW)	Read/Write
$_2B	Input Control System Control Register (ICSYS)	Read/Write[4]
$_2C	Reserved	--
$_2D	Timer Test Register (TIMTST)	Read/Write[2]
$_2E	Precision Timer Prescaler Select Register (PTPSR)	Read/Write
$_2F	Precision Timer Modulus Counter Prescaler Select Register (PTMCPSR)	Read/Write
$_30	16-Bit Pulse Accumulator B Control Register (PBCTL)	Read/Write
$_31	16-Bit Pulse Accumulator B Flag Register (PBFLG)	Read/Write
$_32	8-Bit Pulse Accumulator Holding Register3 (PA3H)	Read/Write[5]
$_33	8-Bit Pulse Accumulator Holding Register2 (PA2H)	Read/Write[5]
$_34	8-Bit Pulse Accumulator Holding Register1 (PA1H)	Read/Write[5]
$_35	8-Bit Pulse Accumulator Holding Register0 (PA0H)	Read/Write[5]
$_36	Modulus Down-Counter Count Register High (MCCNT)	Read/Write

Table 3-1 Module Memory Map

$_37	Modulus Down-Counter Count Register Low (MCCNT)	Read/Write
$_38	Timer Input Capture Holding Register0 High (TC0H)	Read/Write[5]
$_39	Timer Input Capture Holding Register0 Low (TC0H)	Read/Write[5]
$_3A	Timer Input Capture Holding Register1 High(TC1H)	Read/Write[5]
$_3B	Timer Input Capture Holding Register1 Low (TC1H)	Read/Write[5]
$_3C	Timer Input Capture Holding Register2 High (TC2H)	Read/Write[5]
$_3D	Timer Input Capture Holding Register2 Low (TC2H)	Read/Write[5]
$_3E	Timer Input Capture Holding Register3 High (TC3H)	Read/Write[5]
$_3F	Timer Input Capture Holding Register3 Low (TC3H)	Read/Write[5]

1. Always read $00.
2. Only writable in special modes (test_mode = 1).
3. Write to these registers have no meaning or effect during input capture.
4. May be written once when not in test_mode but writes are always permitted when test_mode is enabled.
5. Writes has no effect.

3.3 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

3.3.1 TIOS — Timer Input Capture/Output Compare Select Register

Register offset: $_00

	BIT7	6	5	4	3	2	1	BIT0
R W	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
RESET:	0	0	0	0	0	0	0	0

Figure 3-1 Timer Input Capture/Output Compare Register (TIOS)

Read or write anytime.

All bits reset to zero.

IOS[7:0] — Input Capture or Output Compare Channel Configuration

0 = The corresponding channel acts as an input capture.
1 = The corresponding channel acts as an output compare.

3.3.2 CFORC — Timer Compare Force Register

Register offset: $_01

	BIT7	6	5	4	3	2	1	BIT0
R	0	0	0	0	0	0	0	0
W	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
RESET:	0	0	0	0	0	0	0	0

Figure 3-2 Timer Compare Force Register (CFORC)

Read or write anytime but reads will always return $00 (1 state is transient).

All bits reset to zero.

FOC[7:0] — Force Output Compare Action for Channel 7-0

A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare “x” to occur immediately. The action taken is the same as if a successful comparison had just taken place with the TCx register except the interrupt flag does not get set.

NOTE: *A successful channel 7 output compare overrides any channel 6:0 compares.If a forced output compare on any channel occurs at the same time as the successful output compare then the forced output compare action will take precedence and the interrupt flag will not get set.*

3.3.3 OC7M — Output Compare 7 Mask Register

Register offset: $_02

	BIT7	6	5	4	3	2	1	BIT0
R W	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
RESET:	0	0	0	0	0	0	0	0

Figure 3-3 Output Compare 7 Mask Register (OC7M)

Read or write anytime.

All bits reset to zero.

OC7M[7:0] **—** Output Compare Mask Action for Channel 7-0

0 = The corresponding OC7Dx bit in the Output Compare 7 Data register will not be transferred to the timer port on a successful channel 7 output compare even if the corresponding pin is setup for output compare.

1 = The corresponding OC7Dx bit in the Output Compare 7 Data register will be transferred to the timer port on a successful channel 7 output compare.

***NOTE**: The corresponding channel must also be setup for output compare (IOSx=1) for data to be transferred from the Output Compare 7 Data Register to the timer port.*

3.3.4 OC7D — Output Compare 7 Data Register

Register offset: $_03

	BIT7	6	5	4	3	2	1	BIT0
R W	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
RESET:	0	0	0	0	0	0	0	0

Figure 3-4 Output Compare 7 Data Register (OC7D)

Read or write anytime.

All bits reset to zero.

A channel 7 output compare can cause bits in the output compare 7 data register to transfer to the timer port data register depending on the output compare 7 mask register.

3.3.5 TCNT — Timer Count Register

Register offset: $_04-$_05

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R W	tcnt 15	tcnt 14	tcnt 13	tcnt 12	tcnt 11	tcnt 10	tcnt 9	tcnt 8	tcnt 7	tcnt 6	tcnt 5	tcnt 4	tcnt 3	tcnt 2	tcnt 1	tcnt 0
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 3-5 Timer Count Register (TCNT)

Read anytime and writes have no meaning or effect.

All bits reset to zero.

The 16-bit main timer is an up counter. A read to this register will return the current value of the counter. Access to the counter register will take place in one clock cycle.

***NOTE:** A separate read/write for high byte and low byte in test mode will give a different result than accessing them as a word. The period of the first count after a write to the TCNT registers may be a different size because the write is not synchronized with the prescaler clock.*

3.3.6 TSCR1 — Timer System Control Register 1

Register offset: $_06

	BIT7	6	5	4	3	2	1	BIT0
R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6 Timer System Control Register 1 (TSCR1)

Read or write anytime except PRNT bit is write once.All bits reset to zero.

TEN — Timer Enable

0 = Disables the main timer, including the counter. Can be used for reducing power consumption.
1 = Allows the timer to function normally.

If for any reason the timer is not active, there is no ÷64 clock for the pulse accumulator since the ÷64 is generated by the timer prescaler.

TSWAI — Timer Module Stops While in Wait

0 = Allows the timer module to continue running during wait.
1 = Disables the timer counter, pulse accumualtors and modulus down counter when the MCU is in wait mode. Timer interrupts cannot be used to get the MCU out of wait.

TSFRZ — Timer and Modulus Counter Stop While in Freeze Mode

0 = Allows the timer and modulus counter to continue running while in freeze mode.
1 = Disables the timer and modulus counter whenever the MCU is in freeze mode. This is useful for emulation. The pulse accumulators do not stop in freeze mode.

TFFCA — Timer Fast Flag Clear All

0 = Allows the timer flag clearing to function normally.
1 = A read from an input capture or a write to the output compare channel registers causes the corresponding channel flag, CxF, to be cleared in the TFLG1 register. Any access to the TCNT register clears the TOF flag in the TFLG2 register. Any access to the PACN3 and PACN2 registers clears the PAOVF and PAIF flags in the PAFLG register. Any access to the PACN1 and PACN0 registers clears the PBOVF flag in the PBFLG register. Any access to the MCCNT register clears the MCZF flag in the MCFLG register. This has the advantage of eliminating software overhead in a separate clear sequence. Extra care is required to avoid accidental flag clearing due to unintended accesses.

NOTE: *The flags cannot be cleared via the normal flag clearing mechanism (writing a one to the flag) when TFFCA=1.*

PRNT — Precision Timer

0 = Enables legacy timer. Only bitsDLY0 and DLY1 of the DLYCT register are used for the delay selection of the delay counter. PR0, PR1 and PR2 bits of the TSCR2 register are used for timer counter prescaler selection. MCPR0 and MCPR1 bits of the MCCTL register are used for modulus down counter prescaler selection.

1 = Enables precision timer. All bits in the DLYCT register are used for the delay selection,all bits of the PTPSR register are used for Precision Timer Prescaler Selection and all bits of PTMCPSR register are used for the prescalerPrecision Timer Modulus Counter Prescaler selection.

3.3.7 TTOV — Timer Toggle On Overflow Register 1

Register offset: $_07

	BIT7	6	5	4	3	2	1	BIT0
R W	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
RESET:	0	0	0	0	0	0	0	0

Figure 3-7 Timer Toggle On Overflow Register 1 (TTOV)

Read or write anytime.

All bits reset to zero.

TOVx — Toggle On Overflow Bits

TOVx toggles output compare pin on timer counter overflow. This feature only takes effect when in output compare mode. When set, it takes precedence over forced output compare but not channel 7 override events.

0 = Toggle output compare pin on overflow feature disabled.

1 = Toggle output compare pin on overflow feature enabled.

3.3.8 TCTL1/TCTL2 — Timer Control Register 1/Timer Control Register 2

Register offset:$_08

	BIT7	6	5	4	3	2	1	BIT0
R W	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
RESET	0	0	0	0	0	0	0	0

Register offset:$_09

	BIT7	6	5	4	3	2	1	BIT0
R W	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
RESET	0	0	0	0	0	0	0	0

Figure 3-8 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)

Read or write anytime.

All bits reset to zero.

OMx — Output Mode

OLx — Output Level

These eight pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is one, the pin associated with OCx becomes an output tied to OCx.

Table 3-2 Compare Result Output Action

OMx	OLx	Action
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

NOTE: *To enable output action by OMx and OLx bits on timer port, the corresponding bit in OC7M should be cleared.*

3.3.9 TCTL3/TCTL4 — Timer Control Register 3/Timer Control Register 4

Register offset: $_0A

	BIT7	6	5	4	3	2	1	BIT0
R W	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
RESET:	0	0	0	0	0	0	0	0

Register offset: $_0B

	BIT7	6	5	4	3	2	1	BIT0
R W	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
RESET:	0	0	0	0	0	0	0	0

Figure 3-9 Timer Control Register 3/Timer Control Register 4 (TCTL3/TCTL4)

Read or write anytime.

All bits reset to zero.

EDGxB, EDGxA — Input Capture Edge Control

These eight pairs of control bits configure the input capture edge detector circuits for each input capture channel. The four pairs of control bits in TCTL4 also configure the input capture edge control for the four 8-bit pulse accumulators PAC0-PAC3.EDG0B and EDG0A in TCTL4 also determine the active edge for the 16-bit pulse accumulator PACB.

Table 3-3 Edge Detector Circuit Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

3.3.10 TIE — Timer Interrupt Enable Register

Register offset: $_0C

	BIT7	6	5	4	3	2	1	BIT0
R W	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
RESET:	0	0	0	0	0	0	0	0

Figure 3-10 Timer Interrupt Enable Register (TIE)

Read or write anytime.

All bits reset to zero.

The bits C7I-C0I correspond bit-for-bit with the flags in the TFLG1 status register.

C7I–C0I — Input Capture/Output Compare “x” Interrupt Enable
0 = The corresponding flag is disabled from causing a hardware interrupt.
1 = The corresponding flag is enabled to cause an interrupt.

3.3.11 TSCR2 — Timer System Control Register 2

Register offset: $_0D

	BIT7	6	5	4	3	2	1	BIT0
R	TOI	0	0	0	TCRE	PR2	PR1	PR0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-11 Timer System Control Register 2 (TSCR2)

Read or write anytime.

All bits reset to zero.

TOI — Timer Overflow Interrupt Enable

0 = Timer overflow interrupt disabled.

1 = Hardware interrupt requested when TOF flag set.

TCRE — Timer Counter Reset Enable

This bit allows the timer counter to be reset by a successful channel 7 output compare. This mode of operation is similar to an up-counting modulus counter.

0 = Counter reset disabled and counter free runs.

1 = Counter reset by a successful output compare on channel 7.

NOTE: *If register TC7 = $0000 and TCRE = 1, then the TCNT register will stay at $0000 continuously. If register TC7 = $FFFF and TCRE = 1, the TOF flag will never be set when TCNT is reset from $FFFF to $0000.*

PR2, PR1, PR0 - Timer Prescaler Select

These three bits specify the division rate of the main Timer prescaler when the PRNT bit of register TSCR1 is set to "0". The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

Table 3-4 Prescaler Selection

PR2	PR1	PR0	Prescale Factor
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

3.3.12 TFLG1 — Main Timer Interrupt Flag 1

Register offset: $_0E

	BIT7	6	5	4	3	2	1	BIT0
R W	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
RESET:	0	0	0	0	0	0	0	0

Figure 3-12 Main Timer Interrupt Flag 1 (TFLG1)

Read anytime.

Write used in the flag clearing mechanism. Writing a one to the flag clears the flag. Writing a zero will not affect the current status of the bit.

NOTE: *When TFFCA=1, the flags cannot be cleared via the normal flag clearing mechanism (writing a one to the flag). Reference* **3.3.6 TSCR1 — Timer System Control Register 1**.

All bits reset to zero.

TFLG1 indicates when interrupt conditions have occurred. The flags can be cleared via the normal flag clearing mechanism (writing a one to the flag) or via the fast flag clearing mechanism (Reference TFFCA bit in **3.3.6 TSCR1 — Timer System Control Register 1**).

Use of the TFMOD bit in the ICSYS register in conjunction with the use of the ICOVW register allows a timer interrupt to be generated after capturing two values in the capture and holding registers instead of generating an interrupt for every capture.

C7F–C0F — Input Capture/Output Compare Channel “x” Flag

A CxF flag is set when a corresponding input capture or output compare is detected. C0F can also be set by 16-bit Pulse Accumulator B (PACB). C3F-C0F can also be set by 8-bit pulse accumulators PAC3-PAC0.

If the delay counter is enabled, the CxF flag will not be set until after the delay.

3.3.13 TFLG2 — Main Timer Interrupt Flag 2

Register offset: $_0F

	BIT7	6	5	4	3	2	1	BIT0
R	TOF	0	0	0	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-13 Main Timer Interrupt Flag 2 (TFLG2)

Read anytime.

Write used in the flag clearing mechanism. Writing a one to the flag clears the flag. Writing a zero will not affect the current status of the bit.

NOTE: *When TFFCA=1, the flag cannot be cleared via the normal flag clearing mechanism (writing a one to the flag). Reference* **3.3.6 TSCR1 — Timer System Control Register 1**.

All bits reset to zero.

TFLG2 indicates when interrupt conditions have occurred. The flag can be cleared via the normal flag clearing mechanism (writing a one to the flag) or via the fast flag clearing mechanism (Reference TFFCA bit in **3.3.6 TSCR1 — Timer System Control Register 1**).

TOF — Timer Overflow Flag

Set when 16-bit free-running timer overflows from $FFFF to $0000.

3.3.14 Timer Input Capture/Output Compare Registers 0-7

TC0 — Timer Input Capture/Output Compare Register 0 **Register offset: $_10–$_11**

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0	tc0
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC1 — Timer Input Capture/Output Compare Register 1 **Register offset: $_12–$_13**

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	tc1	tc1	tc1	tc1	tc1	tc1	tc1	tc1	tc1	tc1	tc1	tc1	tc1	tc1	tc1	tc1
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC2 — Timer Input Capture/Output Compare Register 2 **Register offset: $_14–$_15**

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	tc2	tc2	tc2	tc2	tc2	tc2	tc2	tc2	tc2	tc2	tc2	tc2	tc2	tc2	tc2	tc2
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC3 — Timer Input Capture/Output Compare Register 3 **Register offset: $_16–$_17**

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	tc3	tc3	tc3	tc3	tc3	tc3	tc3	tc3	tc3	tc3	tc3	tc3	tc3	tc3	tc3	tc3
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC4 — Timer Input Capture/Output Compare Register 4 **Register offset: $_18–$_19**

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4	tc4
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC5 — Timer Input Capture/Output Compare Register 5 **Register offset: $_1A–$_1B**

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5	tc5
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC6 — Timer Input Capture/Output Compare Register 6 **Register offset: $_1C–$_1D**

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6	tc6
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TC7 — Timer Input Capture/Output Compare Register 7 **Register offset: $_1E–$_1F**

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7	tc7
W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 3-14 Timer Input Capture/Output Compare Registers 0-7

Read anytime.

Write anytime for output compare function. Writes to these registers have no meaning or effect during input capture.

All bits reset to zero.

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

3.3.15 PACTL — 16-Bit Pulse Accumulator A Control Register

Register offset: $_20

	BIT7	6	5	4	3	2	1	BIT0
R	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-15 16-Bit Pulse Accumulator Control Register (PACTL)

Read or write any time

All bits reset to zero.

PAEN — Pulse Accumulator A System Enable

0 = 16-Bit Pulse Accumulator A system disabled. 8-bit PAC3 and PAC2 can be enabled when their related enable bits in ICPAR are set.
Pulse Accumulator Input Edge Flag (PAIF) function is disabled.

1 = 16-Bit Pulse Accumulator A system enabled. The two 8-bit pulse accumulators PAC3 and PAC2 are cascaded to form the PACA 16-bit pulse accumulator. When PACA in enabled, the PACN3 and PACN2 registers contents are respectively the high and low byte of the PACA. PA3EN and PA2EN control bits in ICPAR have no effect.
Pulse Accumulator Input Edge Flag (PAIF) function is enabled.
The PACA shares the input pin with IC7.

PAEN is independent from TEN. With timer disabled, the pulse accumulator can still function unless pulse accumulator is disabled.

PAMOD — Pulse Accumulator Mode

This bit is active only when the Pulse Accumulator A is enabled (PAEN = 1).
0 = event counter mode
1 = gated time accumulation mode

PEDGE — Pulse Accumulator Edge Control

This bit is active only when the Pulse Accumulator A is enabled (PAEN = 1).

For PAMOD bit = 0 (event counter mode).
0 = falling edges on PT7 pin cause the count to be incremented
1 = rising edges on PT7 pin cause the count to be incremented

For PAMOD bit = 1 (gated time accumulation mode).
0 = PT7 input pin high enables bus clock divided by 64 to Pulse Accumulator and the trailing falling edge on PT7 sets the PAIF flag.
1 = PT7 input pin low enables bus clock divided by 64 to Pulse Accumulator and the trailing rising edge on PT7 sets the PAIF flag.

Table 3-5 Pin Action.

PAMOD	PEDGE	Pin Action
0	0	Falling edge
0	1	Rising edge
1	0	Divide by 64 clock enabled with pin high level
1	1	Divide by 64 clock enabled with pin low level

If the timer is not active (TEN = 0 in TSCR1), there is no divide-by-64 since the ÷64 clock is generated by the timer prescaler.

CLK1, CLK0 — Clock Select Bits

Table 3-6 Clock Selection

CLK1	CLK0	Clock Source
0	0	Use timer prescaler clock as timer counter clock
0	1	Use PACLK as input to timer counter clock
1	0	Use PACLK/256 as timer counter clock frequency
1	1	Use PACLK/65536 as timer counter clock frequency

For the description of PACLK please refer to **Figure 4-6**.

If the pulse accumulator is disabled (PAEN = 0), the prescaler clock from the timer is always used as an input clock to the timer counter. The change from one selected clock to the other happens immediately after these bits are written.

PAOVI — Pulse Accumulator A Overflow Interrupt enable
0 = interrupt inhibited
1 = interrupt requested if PAOVF is set

PAI — Pulse Accumulator Input Interrupt enable
0 = interrupt inhibited
1 = interrupt requested if PAIF is set

3.3.16 PAFLG — Pulse Accumulator A Flag Register

Register offset: $_21

	BIT7	6	5	4	3	2	1	BIT0
R	0	0	0	0	0	0	PAOVF	PAIF
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-16 Pulse Accumulator A Flag Register (PAFLG)

Read anytime.

Write used in the flag clearing mechanism. Writing a one to the flag clears the flag. Writing a zero will not affect the current status of the bit.

NOTE: *When TFFCA=1, the flags cannot be cleared via the normal flag clearing mechanism (writing a one to the flag). Reference* **3.3.6 TSCR1 — Timer System Control Register 1**.

All bits reset to zero.

PAFLG indicates when interrupt conditions have occurred. The flags can be cleared via the normal flag clearing mechanism (writing a one to the flag) or via the fast flag clearing mechanism (Reference TFFCA bit in **3.3.6 TSCR1 — Timer System Control Register 1**).

PAOVF — Pulse Accumulator A Overflow Flag

Set when the 16-bit pulse accumulator A overflows from $FFFF to $0000, or when 8-bit pulse accumulator 3 (PAC3) overflows from $FF to $00.

When PACMX=1, PAOVF bit can also be set if 8-bit pulse accumulator 3 (PAC3) reaches $FF followed by an active edge on PT3.

PAIF — Pulse Accumulator Input edge Flag

Set when the selected edge is detected at the PT7 input pin. In event mode the event edge triggers PAIF and in gated time accumulation mode the trailing edge of the gate signal at the PT7 input pin triggers PAIF.

3.3.17 PACN3, PACN2 — Pulse Accumulators Count Registers

Register offset: $_22

	BIT7	6	5	4	3	2	1	BIT0
R W	pacnt7(15)	pacnt6(14)	pacnt5(13)	pacnt4(12)	pacnt3(11)	pacnt2(10)	pacnt1(9)	pacnt0(8)
RESET:	0	0	0	0	0	0	0	0

Figure 3-17 Pulse Accumulators Count Register 3 (PACN3)

Register offset: $_23

	BIT7	6	5	4	3	2	1	BIT0
R W	pacnt7	pacnt6	pacnt5	pacnt4	pacnt3	pacnt2	pacnt1	pacnt0
RESET:	0	0	0	0	0	0	0	0

Figure 3-18 Pulse Accumulators Count Register 2 (PACN2)

Read or write any time.

All bits reset to zero.

The two 8-bit pulse accumulators PAC3 and PAC2 are cascaded to form the PACA 16-bit pulse accumulator. When PACA in enabled (PAEN=1 in PACTL) the PACN3 and PACN2 registers contents are respectively the high and low byte of the PACA.

When PACN3 overflows from $FF to $00, the interrupt flag PAOVF in PAFLG is set.

Full count register access will take place in one clock cycle.

NOTE: *A separate read/write for high byte and low byte will give a different result than accessing them as a word.*

NOTE: *When clocking pulse and write to the registers occurs simultaneously, write takes priority and the register is not incremented.*

3.3.18 PACN1, PACN0 — Pulse Accumulators Count Registers

Register offset: $_24

	BIT7	6	5	4	3	2	1	BIT0
R W	pacnt7(15)	pacnt6(14)	pacnt5(13)	pacnt4(12)	pacnt3(11)	pacnt2(10)	pacnt1(9)	pacnt0(8)
RESET:	0	0	0	0	0	0	0	0

Figure 3-19 Pulse Accumulators Count Register 1 (PACN1)

Register offset: $_25

	BIT7	6	5	4	3	2	1	BIT0
R W	pacnt7	pacnt6	pacnt5	pacnt4	pacnt3	pacnt2	pacnt1	pacnt0
RESET:	0	0	0	0	0	0	0	0

Figure 3-20 Pulse Accumulators Count Register 0 (PACN0)

Read or write any time.

All bits reset to zero.

The two 8-bit pulse accumulators PAC1 and PAC0 are cascaded to form the PACB 16-bit pulse accumulator. When PACB in enabled, (PBEN=1 in PBCTL) the PACN1 and PACN0 registers contents are respectively the high and low byte of the PACB.

When PACN1 overflows from $FF to $00, the interrupt flag PBOVF in PBFLG is set.

Full count register access will take place in one clock cycle.

NOTE: *A separate read/write for high byte and low byte will give a different result than accessing them as a word.*

NOTE: *When clocking pulse and write to the registers occurs simultaneously, write takes priority and the register is not incremented.*

3.3.19 MCCTL — 16-Bit Modulus Down-Counter Control Register

Register offset: $_26

	BIT7	6	5	4	3	2	1	BIT0
R	MCZI	MODMC	RDMCL	0	0	MCEN	MCPR1	MCPR0
W				ICLAT	FLMC			
RESET:	0	0	0	0	0	0	0	0

Figure 3-21 16-Bit Modulus Down-Counter Control Register (MCCTL)

Read or write any time.

All bits reset to zero.

MCZI — Modulus Counter Underflow Interrupt Enable

0 = Modulus counter interrupt is disabled.
1 = Modulus counter interrupt is enabled.

MODMC — Modulus Mode Enable

0 = The modulus counter counts down from the value written to it and will stop at $0000.
1 = Modulus mode is enabled. When the modulus counter reaches $0000, the counter is loaded with the latest value written to the modulus count register.

NOTE: *For proper operation, the MCEN bit should be cleared before modifying the MODMC bit in order to reset the modulus counter to $FFFF.*

RDMCL — Read Modulus Down-Counter Load

0 = Reads of the modulus count register (MCCNT) will return the present value of the count register.
1 = Reads of the modulus count register (MCCNT) will return the contents of the load register.

ICLAT — Input Capture Force Latch Action

When input capture latch mode is enabled (LATQ and BUFEN bit in ICSYS are set), a write one to this bit immediately forces the contents of the input capture registers TC0 to TC3 and their corresponding 8-bit pulse accumulators to be latched into the associated holding registers. The pulse accumulators will be automatically cleared when the latch action occurs.

Writing zero to this bit has no effect. Read of this bit will always return zero.

FLMC — Force Load Register into the Modulus Counter Count Register

This bit is active only when the modulus down-counter is enabled (MCEN=1).

A write one into this bit loads the load register into the modulus counter count register (MCCNT). This also resets the modulus counter prescaler.

Write zero to this bit has no effect.

Read of this bit will return always zero.

MCEN — Modulus Down-Counter Enable

0 = Modulus counter disabled. The modulus counter (MCCNT) is preset to $FFFF. This will prevent an early interrupt flag when the modulus down-counter is enabled.
1 = Modulus counter is enabled.

MCPR1 - MCPR0 — Modulus Counter Prescaler Select

These two bits specify the division rate of the modulus counter prescaler when PRNT of TSCR1 is set to 0. The newly selected prescaler division rate will not be effective until a load of the load register into the modulus counter count register occurs.

Table 3-7 Modulus Counter Prescaler Select

MCPR1	MCPR0	Prescaler division
0	0	1
0	1	4
1	0	8
1	1	16

3.3.20 MCFLG — 16-Bit Modulus Down-Counter FLAG Register

Register offset: $_27

	BIT7	6	5	4	3	2	1	BIT0
R	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-22 16-Bit Modulus Down-Counter FLAG Register (MCFLG)

Read anytime.

Write only used in the flag clearing mechanism for bit 7. Writing a one to bit 7 clears the flag. Writing a zero will not affect the current status of the bit.

NOTE: *When TFFCA=1, the flag cannot be cleared via the normal flag clearing mechanism (writing a one to the flag). Reference* **3.3.6 TSCR1 — Timer System Control Register 1**.

All bits reset to zero.

MCZF — Modulus Counter Underflow Flag

The flag is set when the modulus down-counter reaches $0000.

The flag indicates when interrupt conditions have occurred. The flag can be cleared via the normal flag clearing mechanism (writing a one to the flag) or via the fast flag clearing mechanism (Reference TFFCA bit in **3.3.6 TSCR1 — Timer System Control Register 1**).

POLF3 – POLF0 — First Input Capture Polarity Status

These are read only bits. Writes to these bits have no effect.

Each status bit gives the polarity of the first edge which has caused an input capture to occur after capture latch has been read.

Each POLFx corresponds to a timer PORTx input.

0 = The first input capture has been caused by a falling edge.

1 = The first input capture has been caused by a rising edge.

3.3.21 ICPAR — Input Control Pulse Accumulators Register

Register offset: $_28

	BIT7	6	5	4	3	2	1	BIT0
R	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-23 Input Control Pulse Accumulators Register (ICPAR)

Read or write any time.

All bits reset to zero.

The 8-bit pulse accumulators PAC3 and PAC2 can be enabled only if PAEN in PACTL is cleared. If PAEN is set, PA3EN and PA2EN have no effect.

The 8-bit pulse accumulators PAC1 and PAC0 can be enabled only if PBEN in PBCTL is cleared. If PBEN is set, PA1EN and PA0EN have no effect.

PAxEN — 8-Bit Pulse Accumulator ‘x’ Enable
0 = 8-Bit Pulse Accumulator is disabled.
1 = 8-Bit Pulse Accumulator is enabled.

3.3.22 DLYCT — Delay Counter Control Register

Register offset: $_29

	BIT7	6	5	4	3	2	1	BIT0
R	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-24 Delay Counter Control Register (DLYCT)

Read or write any time.

All bits reset to zero.

DLYx — Delay Counter Select

When the PRNT bit of TSCR1 register is set to 0, only bits DLY0, DLY1 are used to calculate the delay.**Table 3-8** shows the delay settings in this case.

When the PRNT bit of TSCR1 register is set to 1, all bits are used to set a more precise delay. **Table 3-9** shows the delay settings in this case. After detection of a valid edge on an input capture pin, the delay counter counts the pre-selected number of [(dly_cnt + 1)*4]bus clock cycles, then it will generate a pulse on its output if the level of input signal, after the preset delay, is the opposite of the level before the transition.This will avoid reaction to narrow input pulses.

Delay between two active edges of the input signal period should be longer than the selected counter delay.

NOTE: *It is recommended to not write to this register while the timer is enbaled, that is when TEN is set in register TSCR1.*

Table 3-8 Delay Counter Select when PRNT=0

DLY1	DLY0	Delay
0	0	Disabled
0	1	256 bus clock cycles
1	0	512 bus clock cycles
1	1	1024 bus clock cycles

Table 3-9 Delay Counter Select Examples when PRNT=1

DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0	Delay
0	0	0	0	0	0	0	0	Disabled (bypassed)
0	0	0	0	0	0	0	1	8 bus clock cycles
0	0	0	0	0	0	1	0	12 bus clock cycles
0	0	0	0	0	0	1	1	16 bus clock cycles
0	0	0	0	0	1	0	0	20 bus clock cycles
0	0	0	0	0	1	0	1	24 bus clock cycles
0	0	0	0	0	1	1	0	28 bus clock cycles
0	0	0	0	0	1	1	1	32 bus clock cycles
0	0	0	0	1	1	1	1	64 bus clock cycles
0	0	0	1	1	1	1	1	128 bus clock cycles
0	0	1	1	1	1	1	1	256 bus clock cycles
0	1	1	1	1	1	1	1	512 bus clock cycles
1	1	1	1	1	1	1	1	1024 bus clock cycles

3.3.23 ICOVW — Input Control Overwrite Register

Register offset: $_2A

	BIT7	6	5	4	3	2	1	BIT0
R W	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
RESET:	0	0	0	0	0	0	0	0

Figure 3-25 Input Control Overwrite Register (ICOVW)

Read or write any time.

All bits reset to zero.

NOVWx — No Input Capture Overwrite

0 = The contents of the related capture register or holding register can be overwritten when a new input capture or latch occurs.

1 = The related capture register or holding register cannot be written by an event unless they are empty (see **4.2.1 IC Channels**). This will prevent the captured value being overwritten until it is read or latched in the holding register.

3.3.24 ICSYS — Input Control System Control Register

Register offset: $_2B

	BIT7	6	5	4	3	2	1	BIT0
R W	SH37	SH26	SH15	SH04	TFMOD	PACMX	BUFEN	LATQ
RESET:	0	0	0	0	0	0	0	0

Figure 3-26 Input Control System Register (ICSYS)

Read any time

Write once in normal modes.

All bits reset to zero.

SHxy — Share Input action of Input Capture Channels x and y

0 = Normal operation

1 = The channel input ‘x’ causes the same action on the channel ‘y’. The port pin ‘x’ and the corresponding edge detector is used to be active on the channel ‘y’.

TFMOD — Timer Flag-setting Mode

Use of the TFMOD bit in conjunction with the use of the ICOVW register allows a timer interrupt to be generated after capturing two values in the capture and holding registers instead of generating an interrupt for every capture.

By setting TFMOD in queue mode, when NOVWx bit is set and the corresponding capture and holding registers are emptied, an input capture event will first update the related input capture register with the main timer contents. At the next event, the TCx data is transferred to the TCxH register, the TCx is updated and the CxF interrupt flag is set.

In all other input capture cases the interrupt flag is set by a valid external event on PTx.

0 = The timer flags C3F–C0F in TFLG1 are set when a valid input capture transition on the corresponding port pin occurs.

1 = If in queue mode (BUFEN=1 and LATQ=0), the timer flags C3F–C0F in TFLG1 are set only when a latch on the corresponding holding register occurs.
If the queue mode is not engaged, the timer flags C3F–C0F are set the same way as for TFMOD=0.

PACMX — 8-Bit Pulse Accumulators Maximum Count

0 = Normal operation. When the 8-bit pulse accumulator has reached the value $FF, with the next active edge, it will be incremented to $00.

1 = When the 8-bit pulse accumulator has reached the value $FF, it will not be incremented further. The value $FF indicates a count of 255 or more.

BUFEN — IC Buffer Enable

0 = Input Capture and pulse accumulator holding registers are disabled.

1 = Input Capture and pulse accumulator holding registers are enabled. The latching mode is defined by LATQ control bit.

LATQ — Input Control Latch or Queue Mode Enable

The BUFEN control bit should be set in order to enable the IC and pulse accumulators holding registers. Otherwise LATQ latching modes are disabled.

Write one into ICLAT bit in MCCTL, when LATQ and BUFEN are set will produce latching of input capture and pulse accumulators registers into their holding registers.

0 = Queue Mode of Input Capture is enabled.
The main timer value is memorized in the IC register by a valid input pin transition.
With a new occurrence of a capture, the value of the IC register will be transferred to its holding register and the IC register memorizes the new timer value.

1 = Latch Mode is enabled. Latching function occurs when modulus down-counter reaches zero or a zero is written into the count register MCCNT (see **4.2.1.2 Buffered IC Channels**).
With a latching event the contents of IC registers and 8-bit pulse accumulators are transferred to their holding registers. 8-bit pulse accumulators are cleared.

Register offset: $_2D

	BIT7	6	5	4	3	2	1	BIT0
R	0	0	0	0	0	0	TCBYP	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

3.3.25 PTPSR — Precision Timer Prescaler Select Register

Register offset: $_2E

	BIT7	6	5	4	3	2	1	BIT0
R	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-27 Precision Timer Prescaler Select Register (PTPSR)

Read or write any time.

All bits reset to zero.

PTPS7 - PTPS0 — Precision Timer Prescaler Select Bits

These eight bits specify the division rate of the main Timer prescaler. These are effective only when the PRNT bit of TSCR1 is set to 1. **Table 3-10** shows some selection examples in this case.

The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

Table 3-10 Precision Timer Prescaler Selection Examples when PRNT=1

PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0	Prescale Factor
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
0	0	0	0	0	1	0	0	5
0	0	0	0	0	1	0	1	6
0	0	0	0	0	1	1	0	7

PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0	Prescale Factor
0	0	0	0	0	1	1	1	8
0	0	0	0	1	1	1	1	16
0	0	0	1	1	1	1	1	32
0	0	1	1	1	1	1	1	64
0	1	1	1	1	1	1	1	128
1	1	1	1	1	1	1	1	256

3.3.26 PTMCPSR — Precision Timer Modulus Counter Prescaler Select Register

Register offset: $_2F

	BIT7	6	5	4	3	2	1	BIT0
R W	PTMPS7	PTMPS6	PTMPS5	PTMPS4	PTMPS3	PTMPS2	PTMPS1	PTMPS0
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-28 Precision Timer Modulus Counter Prescaler Select Register (PTMCPSR)

Read or write any time.

All bits reset to zero.

PTMPS7 - PTMPS0 — Precision Timer Modulus Counter Prescaler Select bits

These eight bits specify the division rate of the modulus c3.3.31ounter prescaler. These are effective only when the PRNT bit of TSCR1 is set to 1. **Table 3-11** shows some possible division rates.

The newly selected prescaler division rate will not be effective until a load of the load register into the modulus counter count register occurs.

Table 3-11 Precision Timer Modulus Counter Prescaler SelectExamples when PRNT=1

PTMPS7	PTMPS6	PTMPS5	PTMPS4	PTMPS3	PTMPS2	PTMPS1	PTMPS0	Prescaler division rate
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
0	0	0	0	0	1	0	0	5
0	0	0	0	0	1	0	1	6
0	0	0	0	0	1	1	0	7
0	0	0	0	0	1	1	1	8
0	0	0	0	1	1	1	1	16

Table 3-11 Precision Timer Modulus Counter Prescaler SelectExamples when PRNT=1

PTMPS7	PTMPS6	PTMPS5	PTMPS4	PTMPS3	PTMPS2	PTMPS1	PTMPS0	Prescaler division rate
0	0	0	1	1	1	1	1	32
0	0	1	1	1	1	1	1	64
0	1	1	1	1	1	1	1	128
1	1	1	1	1	1	1	1	256

3.3.27 PBCTL — 16-Bit Pulse Accumulator B Control Register

Register offset: $_30

	BIT7	6	5	4	3	2	1	BIT0
R	0	PBEN	0	0	0	0	PBOVI	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-29 16-Bit Pulse Accumulator B Control Register (PBCTL)

Read or write any time.

All bits reset to zero.

PBEN — Pulse Accumulator B System Enable

0 = 16-bit Pulse Accumulator system disabled. 8-bit PAC1 and PAC0 can be enabled when their related enable bits in ICPAR are set.

1 = Pulse Accumulator B system enabled. The two 8-bit pulse accumulators PAC1 and PAC0 are cascaded to form the PACB 16-Bit Pulse Accumulator B. When PACB is enabled, the PACN1 and PACN0 registers contents are respectively the high and low byte of the PACB.
PA1EN and PA0EN control bits in ICPAR have no effect.
The PACB shares the input pin with IC0.

PBEN is independent from TEN. With timer disabled, the pulse accumulator can still function unless pulse accumulator is disabled.

PBOVI — Pulse Accumulator B Overflow Interrupt enable

0 = interrupt inhibited

1 = interrupt requested if PBOVF is set

3.3.28 PBFLG — Pulse Accumulator B Flag Register

Register offset: $_31

	BIT7	6	5	4	3	2	1	BIT0
R	0	0	0	0	0	0	PBOVF	0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-30 Pulse Accumulator B Flag Register (PBFLG)

Read anytime.

Write used in the flag clearing mechanism. Writing a one to the flag clears the flag. Writing a zero will not affect the current status of the bit.

NOTE: *When TFFCA=1, the flag cannot be cleared via the normal flag clearing mechanism (writing a one to the flag). Reference* **3.3.6 TSCR1 — Timer System Control Register 1**.

All bits reset to zero.

PBFLG indicates when interrupt conditions have occurred. The flag can be cleared via the normal flag clearing mechanism (writing a one to the flag) or via the fast flag clearing mechanism (Reference TFFCA bit in **3.3.6 TSCR1 — Timer System Control Register 1**).

PBOVF — Pulse Accumulator B Overflow Flag

This bit is set when the 16-bit pulse accumulator B overflows from $FFFF to $0000, or when 8-bit pulse accumulator 1 (PAC1) overflows from $FF to $00.

When PACMX=1, PBOVF bit can also be set if 8-bit pulse accumulator 1 (PAC1) reaches $FF and an active edge follows on PT1.

3.3.29 PA3H–PA0H — 8-Bit Pulse Accumulators Holding Registers

Register offset: $_32

	BIT7	6	5	4	3	2	1	BIT0
R	PA3H7	PA3H6	PA3H5	PA3H4	PA3H3	PA3H2	PA3H1	PA3H0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-31 8-Bit Pulse Accumulators Holding Register 3 (PA3H)

Register offset: $_33

	BIT7	6	5	4	3	2	1	BIT0
R	PA2H7	PA2H6	PA2H5	PA2H4	PA2H3	PA2H2	PA2H1	PA2H0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-32 8-Bit Pulse Accumulators Holding Register 2 (PA2H)

Register offset: $_34

	BIT7	6	5	4	3	2	1	BIT0
R	PA1H7	PA1H6	PA1H5	PA1H4	PA1H3	PA1H2	PA1H1	PA1H0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-33 8-Bit Pulse Accumulators Holding Register 1 (PA1H)

Register offset: $_35

	BIT7	6	5	4	3	2	1	BIT0
R	PA0H7	PA0H6	PA0H5	PA0H4	PA0H3	PA0H2	PA0H1	PA0H0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-34 8-Bit Pulse Accumulators Holding Register 0 (PA0H)

Read any time.

Write has no effect.

All bits reset to zero.

These registers are used to latch the value of the corresponding pulse accumulator when the related bits in register ICPAR are enabled (see **4.2.3 Pulse Accumulators**).

3.3.30 MCCNT — Modulus Down-Counter Count Register

Register address:$_36-$_37

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R W	mccnt 15	mccnt 14	mccnt 13	mccnt 12	mccnt 11	mccnt 10	mccnt 9	mccnt 8	mccnt 7	mccnt 6	mccnt 5	mccnt 4	mccnt 3	mccnt 2	mccnt 1	mccnt 0
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 3-35 Modulus Down-Counter Count Register (MCCNT)

Read or write any time.

All bits reset to one.

A full access for the counter register will take place in one clock cycle.

NOTE: *A separate read/write for high byte and low byte will give different results than accessing them as a word.*

If the RDMCL bit in MCCTL register is cleared, reads of the MCCNT register will return the present value of the count register. If the RDMCL bit is set, reads of the MCCNT will return the contents of the load register.

If a $0000 is written into MCCNT when LATQ and BUFEN in ICSYS register are set, the input capture and pulse accumulator registers will be latched.

With a $0000 write to the MCCNT, the modulus counter will stay at zero and does not set the MCZF flag in MCFLG register.

If the modulus down counter is enabled (MCEN=1) and modulus mode is enabled (MODMC=1), a write to MCCNT will update the load register with the value written to it. The count register will not be updated with the new value until the next counter underflow.

If modulus mode is not enabled (MODMC=0), a write to MCCNT will clear the modulus prescaler and will immediately update the counter register with the value written to it and down-counts to $0000 and stops.

The FLMC bit in MCCTL can be used to immediately update the count register with the new value if an immediate load is desired.

3.3.31 Timer Input Capture Holding Registers 0-3

Register offset: $_38-$_39

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-36 Timer Input Capture Holding Register 0 (TC0H)

Register offset: $_3A-$_3B

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-37 Timer Input Capture Holding Register 1 (TC1H)

Register offset: $_3C-$_3D

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-38 Timer Input Capture Holding Register 2 (TC2H)

Register offset: $_3E-$_3F

	BIT15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT0
R	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
W																
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-39 Timer Input Capture Holding Register 3 (TC3H)

Read any time

Write has no effect.

All bits reset to zero.

These registers are used to latch the value of the input capture registers TC0 – TC3. The corresponding IOSx bits in TIOS should be cleared (see **4.2.1 IC Channels**).

Section 4 Functional Description

4.1 General

This section provides a complete functional description of the ECT block, detailing the operation of the design from the end user perspective in a number of subsections.

Figure 4-1 Detailed Timer Block Diagram in Latch Mode when PRNT=0

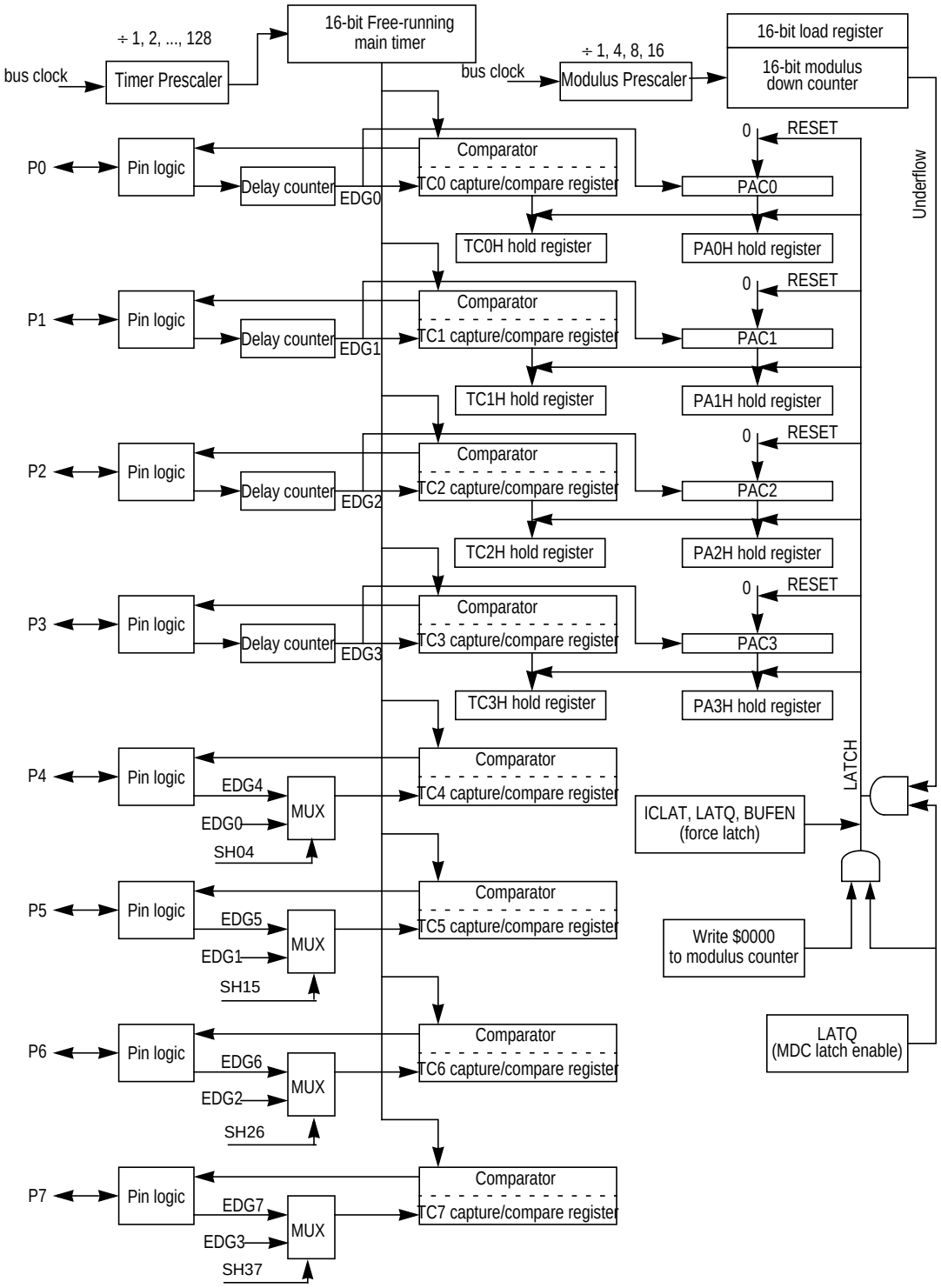


Figure 4-2 Detailed Timer Block Diagram in Latch Mode when PRNT=1

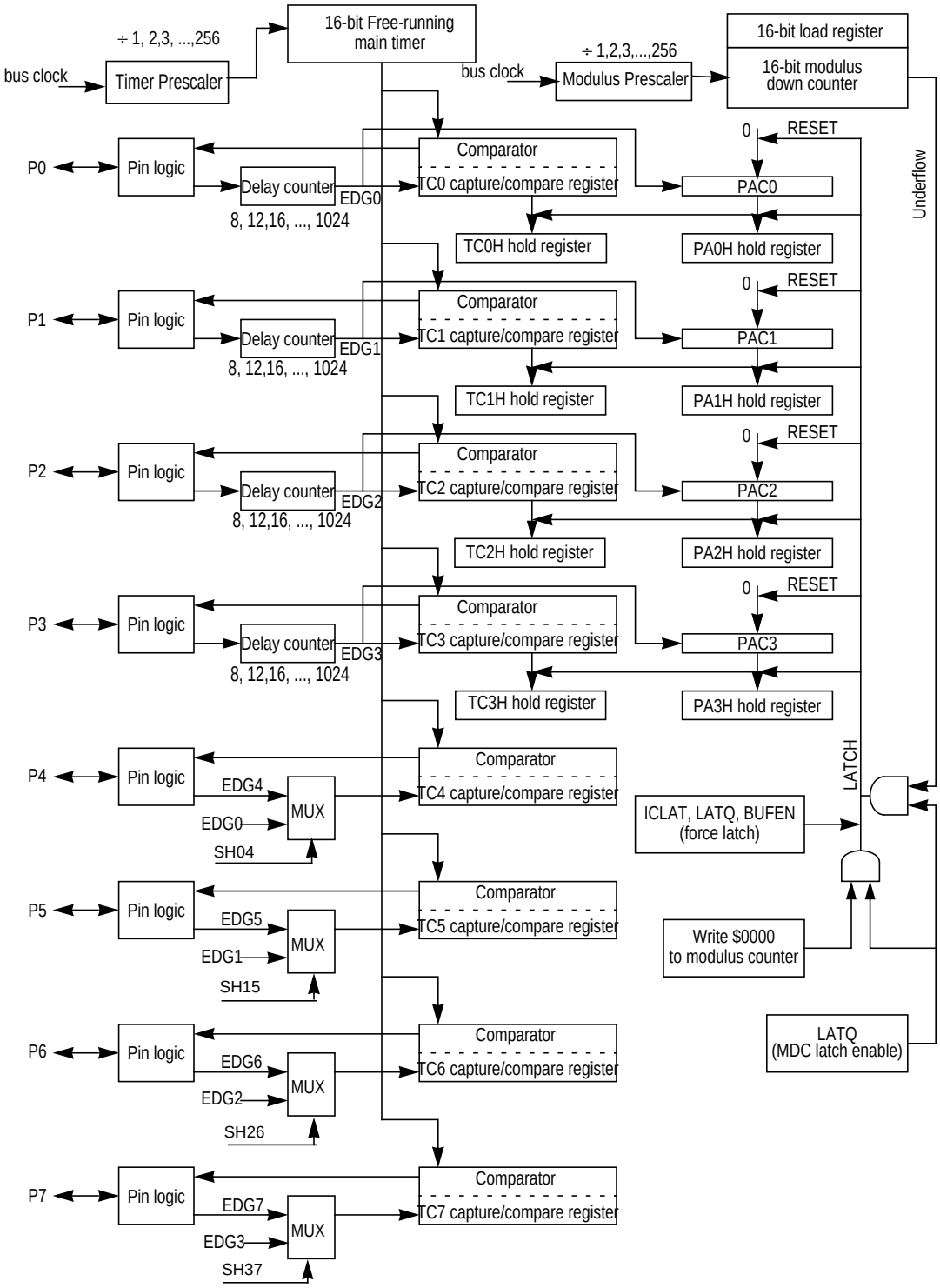


Figure 4-3 Detailed Timer Block Diagram in Queue Mode when PRNT=0

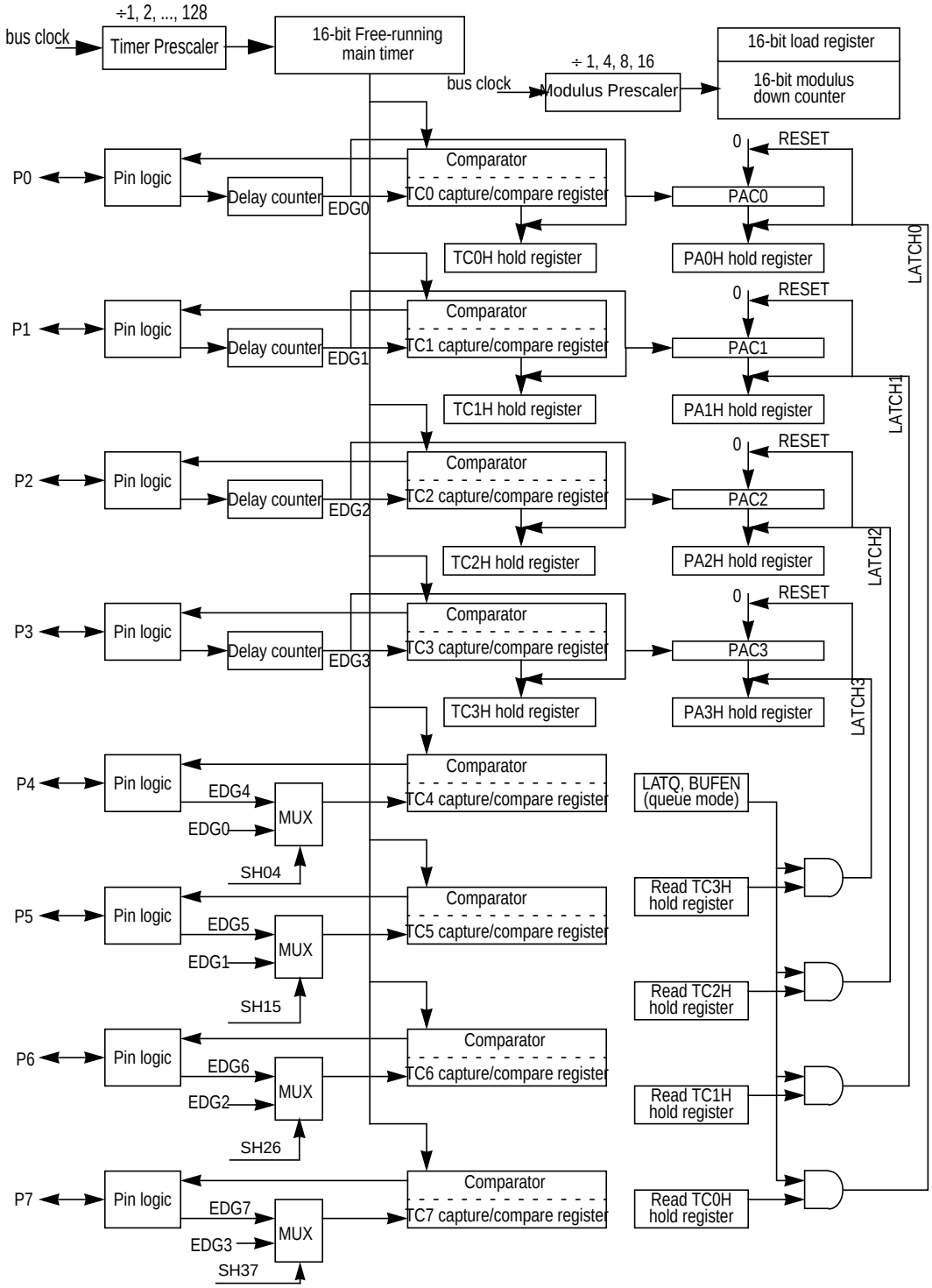


Figure 4-4 Detailed Timer Block Diagram in Queue Mode when PRNT=1

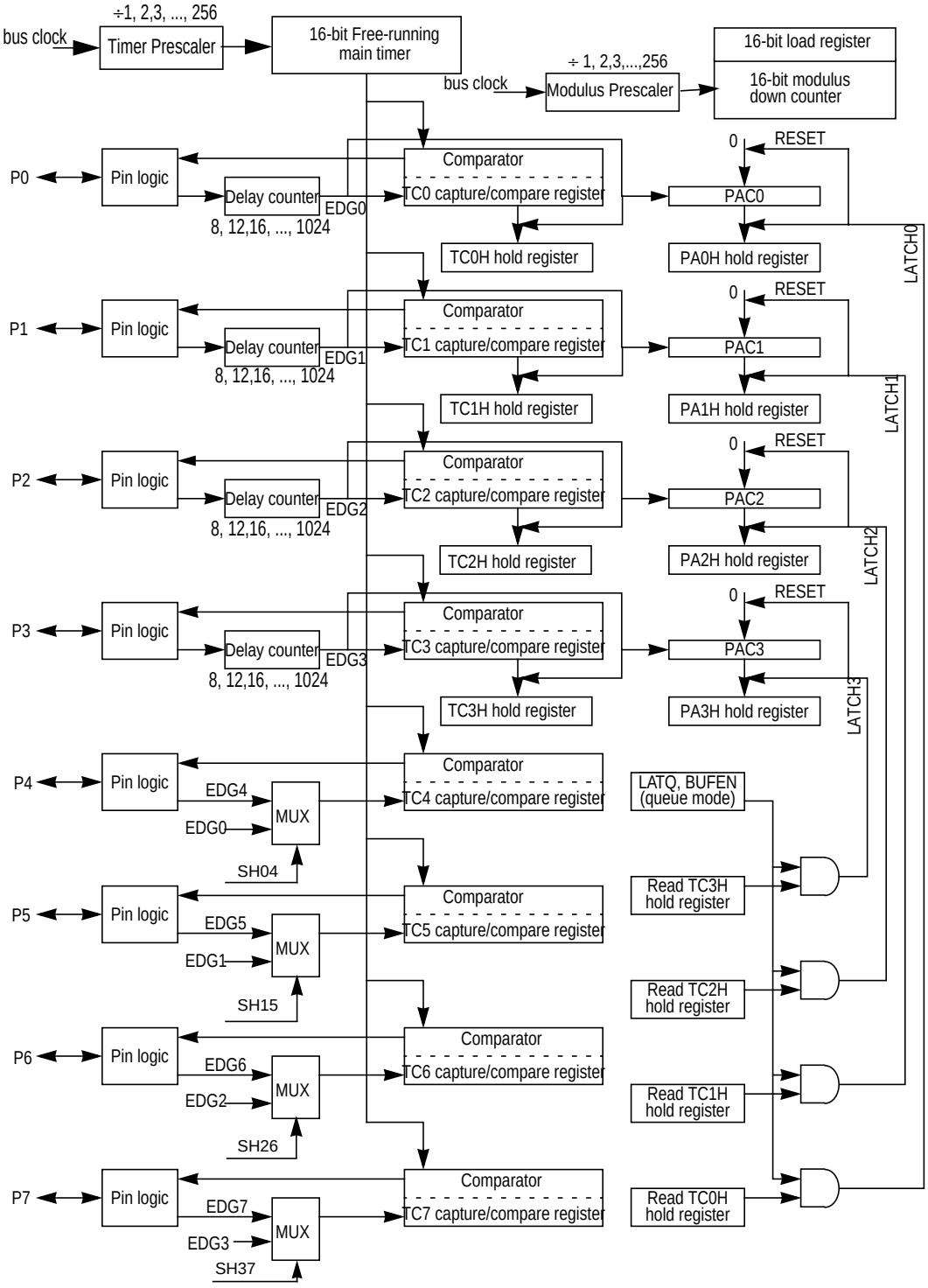


Figure 4-5 8-Bit Pulse Accumulators Block Diagram

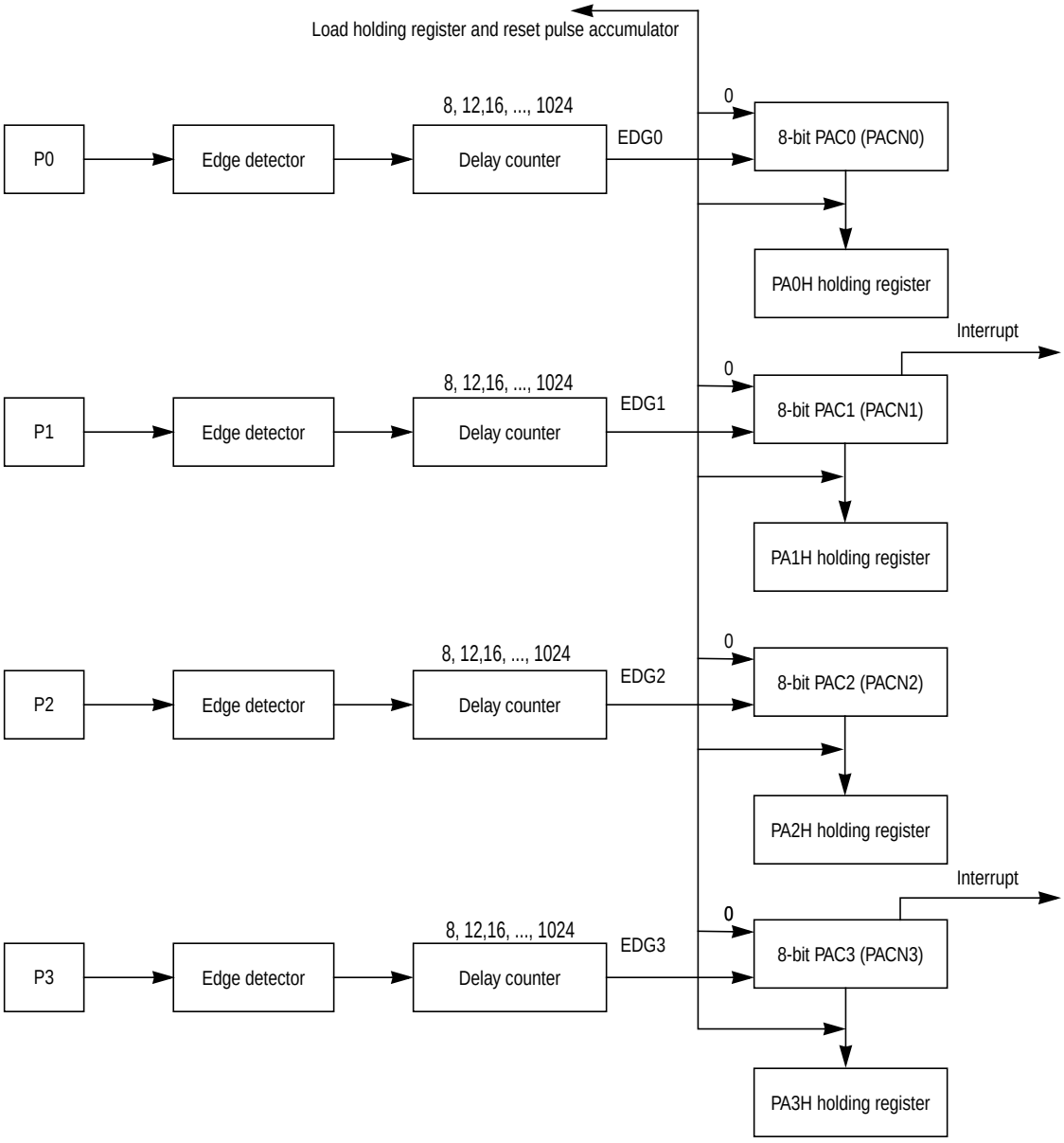


Figure 4-6 16-Bit Pulse Accumulators Block Diagram

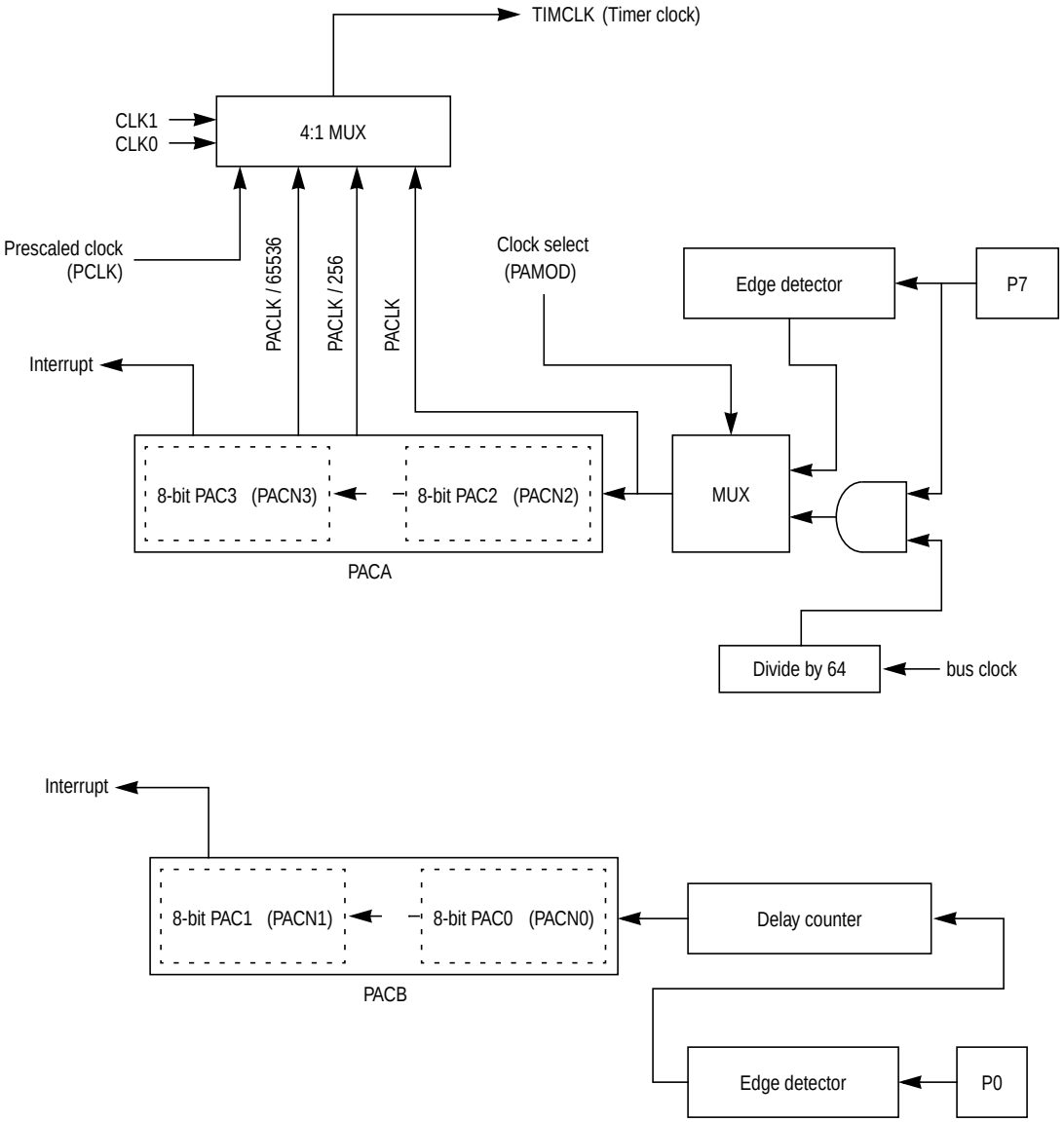
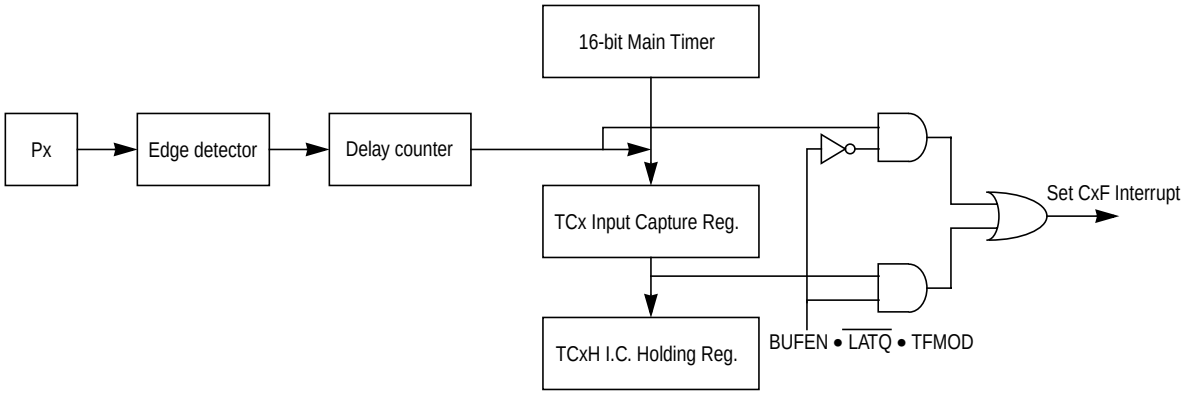


Figure 4-7 Block Diagram for Port 7 with Output Compare/Pulse Accumulator A



4.2 Enhanced Capture Timer Modes of Operation

The Enhanced Capture Timer has 8 Input Capture, Output Compare (IC/OC) channels same as on the HC12 standard timer (timer channels TC0 to TC7). When channels are selected as input capture by selecting the IOSx bit in TIOS register, they are called Input Capture (IC) channels.

Four IC channels (channels 7-4) are the same as on the standard timer with one capture register each which memorizes the timer value captured by an action on the associated input pin.

Four other IC channels (channels 3-0), in addition to the capture register, also have one buffer each called a holding register. This allows two different timer values to be saved without generating any interrupts.

Four 8-bit pulse accumulators are associated with the four buffered IC channels (channels 3-0). Each pulse accumulator has a holding register to memorize their value by an action on its external input. Each pair of pulse accumulators can be used as a 16-bit pulse accumulator.

The 16-bit modulus down-counter can control the transfer of the IC registers and the pulse accumulators contents to the respective holding registers for a given period, every time the count reaches zero.

The modulus down-counter can also be used as a stand-alone time base with periodic interrupt capability.

4.2.1 IC Channels

The IC channels are composed of four standard IC registers and four buffered IC channels.

An **IC register** is **empty** when it has been read or latched into the holding register.

A **holding register** is **empty** when it has been read.

4.2.1.1 Non-Buffered IC Channels

The main timer value is memorized in the IC register by a valid input pin transition. If the corresponding NOVWx bit of the ICOVW register is cleared, with a new occurrence of a capture, the contents of IC register are overwritten by the new value. If the corresponding NOVWx bit of the ICOVW register is set, the capture register cannot be written unless it is empty. This will prevent the captured value from being overwritten until it is read.

4.2.1.2 Buffered IC Channels

There are two modes of operations for the buffered IC channels:

- IC Latch Mode (LATQ=1)

  The main timer value is memorized in the IC register by a valid input pin transition (see **Figure 4-1** and **Figure 4-2**).

  The value of the buffered IC register is latched to its holding register by the modulus counter for a given period when the count reaches zero, by a write $0000 to the modulus counter or by a write to ICLAT in the MCCTL register.

  If the corresponding NOVWx bit of the ICOVW register is cleared, with a new occurrence of a capture, the contents of IC register are overwritten by the new value. In case of latching, the contents of its holding register are overwritten.

  If the corresponding NOVWx bit of the ICOVW register is set, the capture register or its holding register cannot be written by an event unless they are empty (see **4.2.1**). This will prevent the captured value from being overwritten until it is read or latched in the holding register.

- IC Queue Mode (LATQ=0)

  The main timer value is memorized in the IC register by a valid input pin transition (see **Figure 4-3** and **Figure 4-4**).

  If the corresponding NOVWx bit of the ICOVW register is cleared, with a new occurrence of a capture, the value of the IC register will be transferred to its holding register and the IC register memorizes the new timer value.

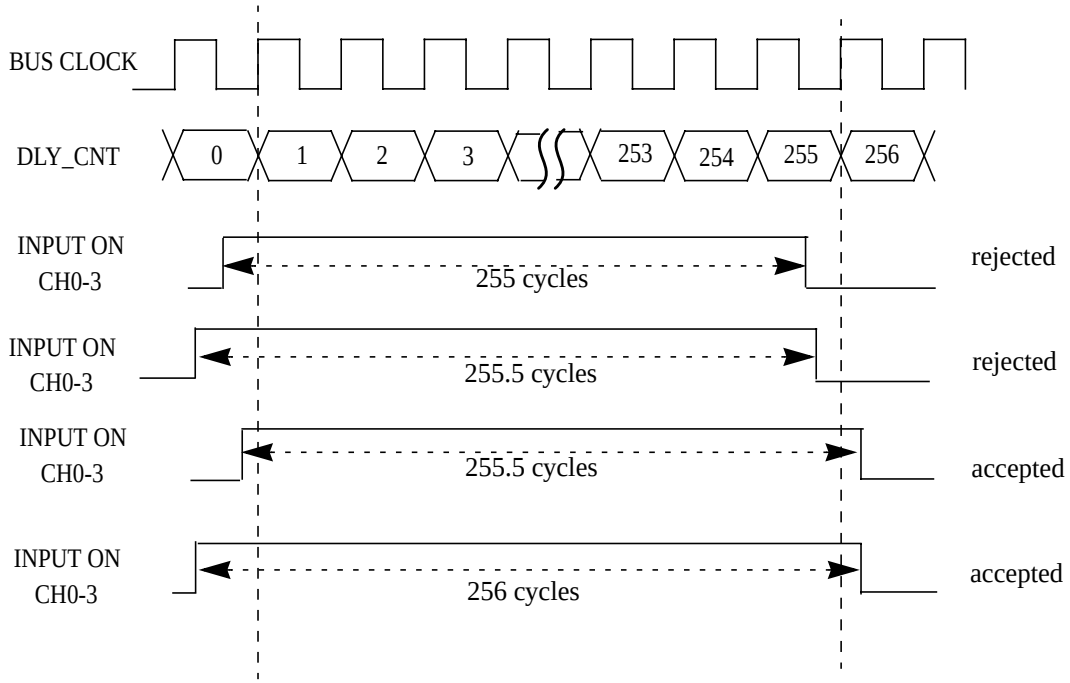
  If the corresponding NOVWx bit of the ICOVW register is set, the capture register or its holding register cannot be written by an event unless they are empty (see **4.2.1**).

  In queue mode, reads of the holding register will latch the corresponding pulse accumulator value to its holding register.

4.2.1.3 Delayed IC channels

There are four delay counters in this module associated with IC channels 0 - 3. The use of this feature is explained in the diagram and notes below.

Figure 4-8 Channel Input validity with delay counter feature



In the diagram above a delay counter value of 256 bus cycles is considered.

1. Input pulses with a duration of (DLY_CNT - 1) cycles or shorter are rejected.
2. Input pulses with a duration between (DLY_CNT - 1) and DLY_CNT cycles may be rejected or accepted, depending on their relative alignment with the sample points.
3. Input pulses with a duration between (DLY_CNT - 1) and DLY_CNT cycles may be rejected or accepted, depending on their relative alignment with the sample points.
4. Input pulses with a duration of DLY_CNT or longer are accepted.

4.2.2 OC channel initialization

Internal register whose output drives OCx when TIOS is set, can be force loaded with a a desired data by writing to CFORC register before OCx is configured for output compare action. This allows a glitch free switch over of port from general purpose I/O to timer ouput once the output compare is enabled.

4.2.3 Pulse Accumulators

There are four 8-bit pulse accumulators with four 8-bit holding registers associated with the four IC buffered channels 3-0. A pulse accumulator counts the number of active edges at the input of its channel.

The minimum pulse width for the PAI input is greater than two bus clocks.The maximum input frequency on the pulse accumulator channel is one half the bus frequency or Eclk.

The user can prevent the 8-bit pulse accumulators from counting further than $FF by utilizing the PACMX control bit in the ICSYS register. In this case, a value of $FF means that 255 counts or more have occurred.

Each pair of pulse accumulators can be used as a 16-bit pulse accumulator (see **Figure 4-6**).

To operate the 16-bit pulse accumulators A and B (PACA and PACB) independently of input capture or output compare 7 and 0 respectively, the user must set the corresponding bits: IOSx=1, OMx=0 and OLx=0. OC7M7 or OC7M0 in the OC7M register must also be cleared.

There are two modes of operation for the pulse accumulators:

- Pulse Accumulator Latch Mode

  The value of the pulse accumulator is transferred to its holding register when the modulus down-counter reaches zero, a write $0000 to the modulus counter or when the force latch control bit ICLAT is written.

  At the same time the pulse accumulator is cleared.

- Pulse Accumulator Queue Mode

  When queue mode is enabled, reads of an input capture holding register will transfer the contents of the associated pulse accumulator to its holding register.

  At the same time the pulse accumulator is cleared.

4.2.4 Modulus Down-Counter

The modulus down-counter can be used as a time base to generate a periodic interrupt. It can also be used to latch the values of the IC registers and the pulse accumulators to their holding registers.

The action of latching can be programmed to be periodic or only once.

4.2.5 Precision Timer

By enabling the PRNT bit of the TSCR1 register, the performance of the timer can be enhanced. In this case, it is possible to set additional prescalar settings for the main timer counter and modulus down counter and enhance delay counter settings compared to the settings in the present ECT timer.

4.2.6 Flag Clearing Mechanisms

The flags in the ECT can be cleared one of two ways:

- Normal Flag Clearing Mechanism (TFFCA=0)

Any of the ECT flags can be cleared by writing a one to the flag.

- Fast Flag Clearing Mechanism (TFFCA=1)

  With the Timer Fast Flag Clear All (TFFCA) enabled, the ECT flags can only be cleared by accessing the various registers associated with the ECT modes of operation as described below. The flags cannot be cleared via the normal flag clearing mechanism. This fast flag clearing mechanism has the advantage of eliminating the software overhead required by a separate clear sequence. Extra care must be taken to avoid accidental flag clearing due to unintended accesses.

  – Input Capture

    A read from an input capture channel register causes the corresponding channel flag, CxF, to be cleared in the TFLG1 register.

  – Output Compare

    A write to the output compare channel register causes the corresponding channel flag, CxF, to be cleared in the TFLG1 register.

  – Timer Counter

    Any access to the TCNT register clears the TOF flag in the TFLG2 register.

  – Pulse Accumulator A

    Any access to the PACN3 and PACN2 registers clears the PAOVF and PAIF flags in the PAFLG register.

  – Pulse Accumulator B

    Any access to the PACN1 and PACN0 registers clears the PBOVF flag in the PBFLG register.

  – Modulus Down Counter

    Any access to the MCCNT register clears the MCZF flag in the MCFLG register.

Section 5 Reset

5.1 General

The reset state of each individual bit is listed within the Register Description section (**Section 3 Memory Map and Registers**)which details the registers and their bit-fields.

Section 6 Interrupts

6.1 General

This section describes interrupts originated by the ECT_16B8C block.The MCU must service the interrupt requests. **Table 6-1** lists the interrupts generated by the ECT to communicate with the MCU.

Table 6-1 ECT Interrupts

Interrupt Source	Description
Timer Channel 7-0	Active high timer channel interrupts 7-0
Modulus counter underflow	Active high modulus counter interrupt
Pulse Accumulator B Overflow	Active high pulse accumulator B interrupt
Pulse Accumulator A Input	Active high pulse accumulator A input interrupt
Pulse Accumulator A Overflow	Pulse accumulator overflow interrupt
Timer Overflow	Timer Overflow interrupt

6.2 Description of Interrupt Operation

The ECT_16B8C only originates interrupt requests. The following is a description of how the module makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt number are chip dependent.

6.2.1 Channel [7:0] Interrupt

This active high output will be asserted by the module to request a timer channel 7 - 0 interrupt to be serviced by the system controller.

6.2.2 Modulus Counter Interrupt

This active high output will be asserted by the module to request a modulus counter underflow interrupt to be serviced by the system controller.

6.2.3 Pulse Accumulator B Overflow Interrupt

This active high output will be asserted by the module to request a timer pulse accumulator B overflow interrupt to be serviced by the system controller.

6.2.4 Pulse Accumulator A Input Interrupt

This active high output will be asserted by the module to request a timer pulse accumulator A input interrupt to be serviced by the system controller.

6.2.5 Pulse Accumulator A Overflow Interrupt

This active high output will be asserted by the module to request a timer pulse accumulator A overflow interrupt to be serviced by the system controller.

6.2.6 Timer Overflow Interrupt

This active high output will be asserted by the module to request a timer overflow interrupt to be serviced by the system controller.

User Guide End Sheet

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