Freescale Semiconductor
Application Note

AN2727
Rev. 0, 12/2004

Designing Hardware for the HCS12 D-Family

by: Martyn Gallop
Applications Engineering
Freescale Semiconductor,
East Kilbride

Introduction

This document contains hardware guidelines for designing with the HCS12 D-family of microcontrollers from Freescale Semiconductor. This includes:

- Pinout overview
- Power supply connections
- Control pin connections
- I/O connections

NOTE

Electrical parameters mentioned in this document are subject to change in individual device specifications. Check each application against the latest data sheet for specific target devices.

freescale™ semiconductor

Recommended Documentation

Other documentation useful for HCS12 D-family hardware design can be found on the external Freescale web site (http://www.freescale.com):

Specific Device User Guide.

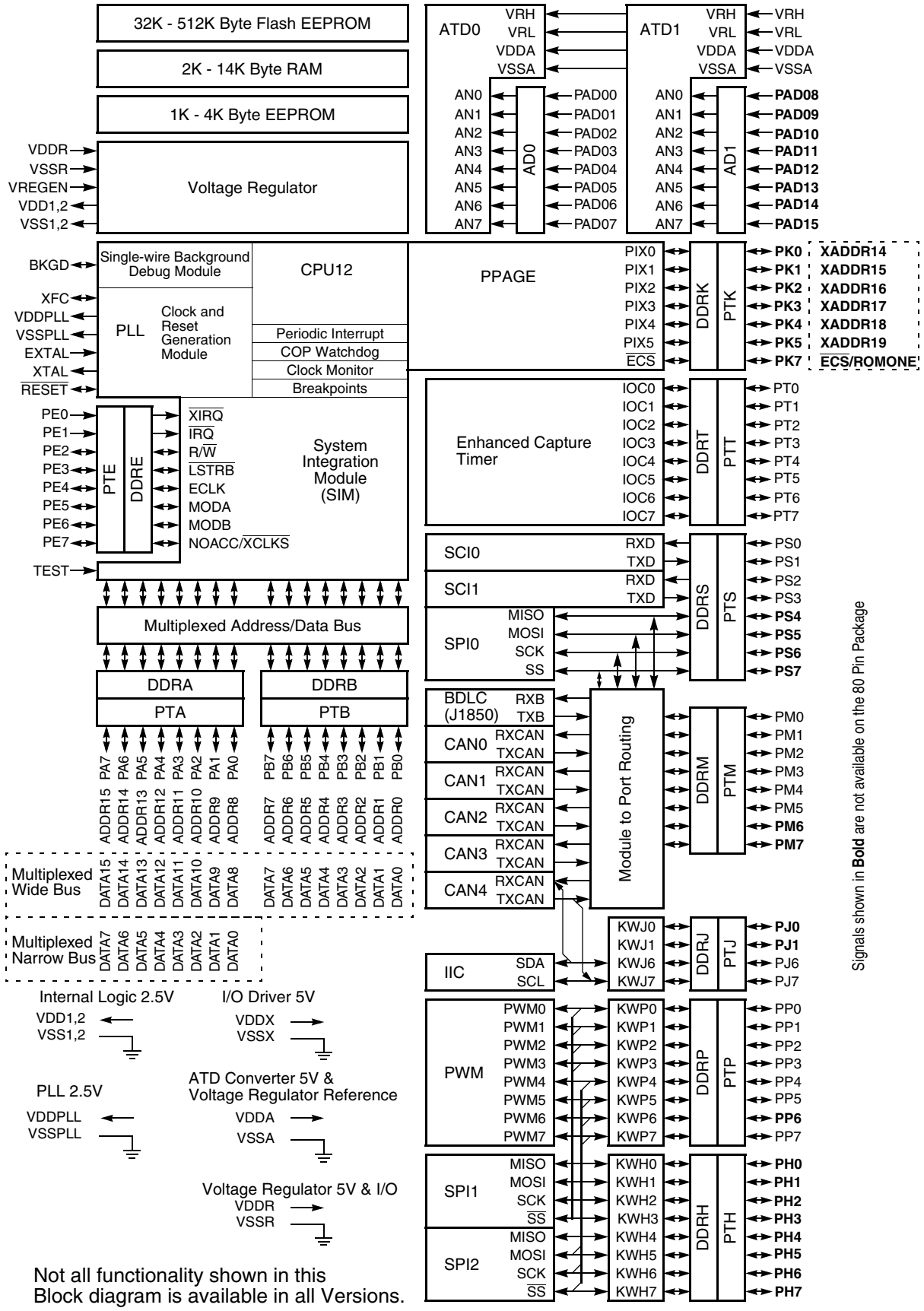
The specific device Voltage Regulator Block User Guide.

The Specific device Port Integration Block User Guide.

Application Note AN2429 “Interfacing to the HCS12 ATD Module.”

Application Note AN2287 “HCS12 External Bus Design.” See also AN2408.

Engineering Bulletin EB386 “HCS12 D-family Compatibility Considerations.”



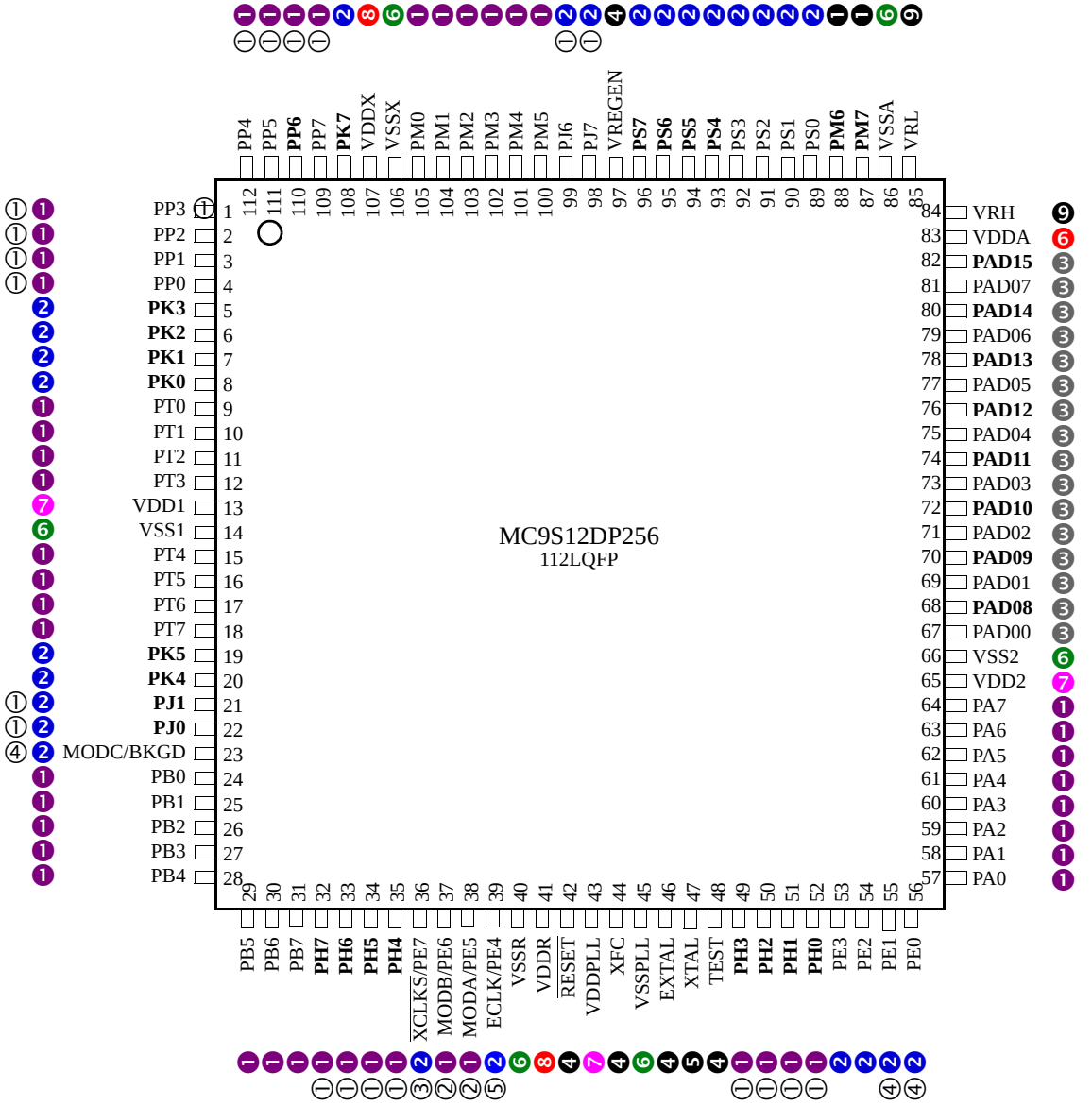
Designing Hardware for the HCS12 D-Family, Rev. 0

Pin States Following Reset in Normal Single Chip Mode

Typically, I/O pins are configured as inputs following a reset; this is done to avoid conflict with application signals driving I/O pins.

Some I/O pins are sampled on reset to determine the reset configuration of the device. These control pins and some GPIO (general purpose input/output) pins have internal pull devices enabled by reset.

The following diagrams show the status of each pin when the device comes out of reset in normal single chip mode.

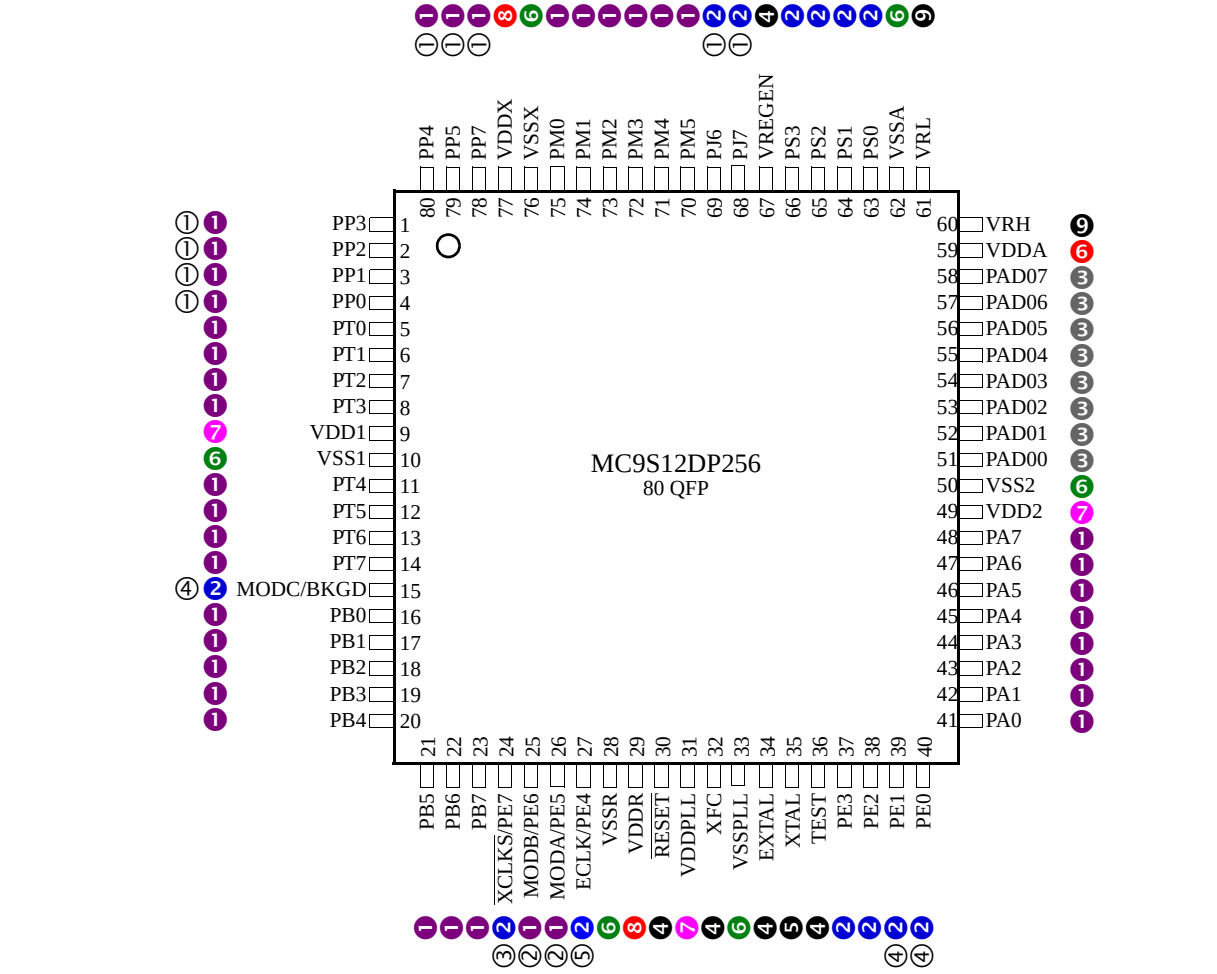


1 = Input, high impedance
2 = Input, internal pull-up enabled
3 = Analog input, high impedance, tie to ground if not used
4 = Control, always connect
5 = Connect if using internal oscillator
6 = 0V
7 = 2.5V supply
8 = 5V supply
9 = ATD reference

Always connect to appropriate voltages and/or decoupling

① = Pin has key wake-up capability
② = Internal pull-downs active only during reset
③ = Pin is sampled at reset for oscillator selection
④ = Pin always has internal pull-up
⑤ = Pin is ECLK output in special modes

Figure 1. S12 D-family 112LQFP Pin State Out of Reset in Normal Single Chip Mode



1 = Input, high impedance
2 = Input, internal pull-up enabled
3 = Analog input, high impedance, tie to ground if not used
4 = Control, always connect
5 = Connect if using internal oscillator
6 = 0V
7 = 2.5V supply
8 = 5V supply
9 = ATD reference

Always connect to appropriate voltages and/or decoupling

① = Pin has key wake-up capability
② = Internal pull-downs active only during reset
③ = Pin is sampled at reset for oscillator selection
④ = Pin always has internal pull-up
⑤ = Pin is ECLK output in special modes

Figure 2. S12 D-family 80QFP Pin State Out of Reset in Normal Single Chip Mode

Power Supply Considerations

There are two power supply voltages:

- 2.5V supply for logic, the CPU core, PLL, and oscillator,
- 5V supply (VDD5) for the I/O buffers, voltage regulator, and ATD.

In some cases, the different supplies may be connected internally on the chip by ESD protection diodes but these connections are not intended for power distribution. Each pair of supply pins must be considered individually and **all power supply pins must be connected appropriately on the PCB.**

The core must not be powered down separately from the I/O.

The 5V supply must not be switched off while the core is powered from an external 2.5V supply.

When using the internal voltage regulator, the 2.5V supply pins (VDD1, VDD2 and VDDPLL) should not be connected together on the pcb. They should be connected only to appropriate decoupling capacitors. **The internal voltage regulator is not designed to supply external circuitry.**

When using an external voltage regulator, the 2.5V supply pins must be connected on the PCB with decoupling capacitors close to each supply pin pair — take steps to keep the VDDPLL supply clean from noise.

The PCB must be carefully laid out to ensure optimal operation of the internal voltage regulator as well as of the MCU itself. In general, it is advisable to route the MCU power and oscillator first. A recommended layout can be found in the Voltage Regulator section of the relevant Device User Guide.

Power Supply Layout Guidelines

Every supply pair must be decoupled by a ceramic capacitor, preferably surface mount, connected as close as possible to the corresponding pins. Keep the decoupling capacitors on the same side of the PCB as the MCU with no vias in the connections from the decoupling capacitor to the MCU pins.

Use low impedance connections to VSS1, VSS2, and VSSR. If not using a full board ground plane, connect the ground pins in a star arrangement with the central point of the ground star at the VSSR pin. Where there is a full board ground plane, connect all VSS supplies directly to the plane, except for VSSPLL and the oscillator circuit ground.

Connect VSSPLL directly to VSSR (maintaining the star layout).

The example layout in the Device User guides shows a copper fill under the MCU, connecting the grounds, with exclusion slots in the fill. The intent is to provide low impedance connectivity with a star configuration.

In general, the oscillator ground return should be considered as a separate ground, routed directly back to VSSPLL and not connected elsewhere to the digital ground. The TEST pin is a static logic input that can also be connected to the oscillator ground to facilitate oscillator layout and minimize the impedance of the oscillator ground.

HCS12 Power Supplies

Vdd1, Vdd2

2.5V supply for MCU core and peripheral logic.

If using the internal regulator, connect only to external decoupling capacitors.

Vddpll

2.5V supply for oscillator and PLL.

If using the internal regulator, connect only to external decoupling capacitor.

Vddr

Supply for regulator and ports A,B,E,H. Connect to VDD5.

Add 10 µF if big loads are switched.

Vddx

Supply for all other ports. Connect to VDD5.

Add 10 µF if big loads are switched.

Vdda

Supply to ATD, Port ADx and voltage regulator reference. Connect to VDD5.

Where possible, avoid connecting external pull devices or logic to VDDA or VSSA tracks.

Vrh

Reference for ATD. Connect to ATD reference potential.

The following constraint must be met to obtain full-scale, full-range ATD results:

$VSSA \leq VRL \leq VIN \leq VRH \leq VDDA$.

If the input level goes outside this range it will be clipped.

VRH should always be $\leq$ VDDA, to maintain conversion accuracy.

Avoid tracking the reference voltage through digital supply planes, and do not connect external digital pull devices to VRH or VRL.

In extreme cases, where high frequency system noise is present, low ESR[1] series inductors and/or ferrite beads may be necessary on VRH. Series resistance should be avoided, as each ATD reference draws ~375 µA from the reference supply (VRH=5V).

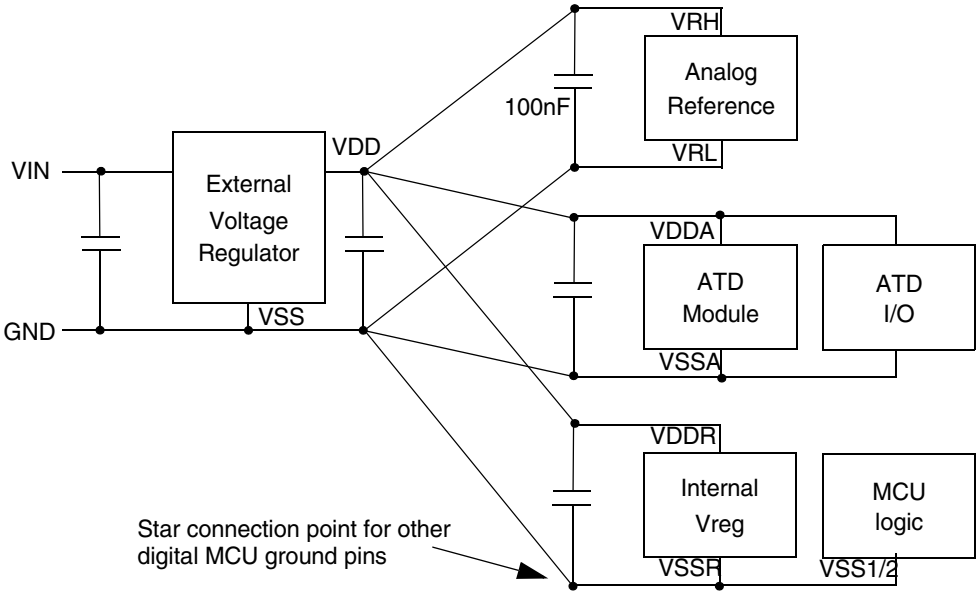
Ground

The oscillator return should be directly to VSSPLL, which should in turn be connected to all other digital grounds via a low impedance ground plane (preferred) or a ‘star’ configuration centred at VSSR.

The oscillator ground should not be otherwise connected to the digital ground.

Vssa, Vssr

Where ATD accuracy is important, these should star separately from the external voltage regulator or voltage source.



1. Equivalent series resistance.

Pin Considerations Collection – Control

There are several control pins on the device that require special consideration at the design stage:

TEST Pin

This pin should always be grounded in an application.

This is a digital input and presents a static load; it can, therefore, be connected to the oscillator ground return without concern.

$\overline{\text{RESET}}$ Pin

This is an open-drain, active-low, bidirectional control pin. It requires an external pull-up.

On assertion of any reset, the MCU releases internal control of the reset pin after 128 SYSCLK cycles, and then samples the reset pin after a further 64 SYSCLK cycles. If the pin reads low, the MCU determines that this was an external reset request and takes the external/POR reset vector. If it reads high, the MCU tests the internal reset sources and takes the appropriate reset vector.

If the time constant of external devices connected to the reset pin is too long, an internally generated reset may be detected as an external reset. If the desired application reset behavior is the same for all reset sources, this is not an issue; however, some applications may require different behavior for different reset sources.

To guarantee that the internal reset vectors (COP and CM) can be recognized by the reset logic then the rise time for the reset pin to reach 3.25V (a guaranteed input logic 1 for VDD5 = 5V) must be less than 64 oscillator (SYSCLK) cycles AND less than 11 µs (64 f_{SCM} cycles @ 5.5 MHz).

There is no LVR[1] support on the HCS12 D-family. It is recommended to use an external LVR circuit to hold the device in reset if the VVD5 supply drops below 4.5V.

Port E.7 : $\overline{\text{XCLKS}}$ Pin

This is a GPIO pin that is also used to control the oscillator configuration on reset.

The $\overline{\text{XCLKS}}$ state is latched at the rising edge of reset, so it important that the logic state of this pin be clearly defined on release of reset.

If the input is a logic low, the oscillator is configured for an external clock drive on EXTAL or as a Pierce Oscillator (not available on MC9S12D256x K36N and K79X masks). If this input is a logic high, a Colpitts oscillator circuit is configured on EXTAL and XTAL.

1. Low voltage reset.

CAUTION

Take care reading the documentation when determining the polarity of the $\overline{XCLKS}$ pin. It is possible for different HCS12 families to have alternative polarity on this pin for oscillator selection. The block user guide for the oscillator refers to the XCLKS signal; this is an active high signal. On the D-family, the pin is $\overline{XCLKS}$, an active low input, which must be pulled low to assert the XCLKS signal to the oscillator module.

The logic level must be clearly defined at reset to select the oscillator configuration appropriate to the external oscillator component layout. This is a common cause of unexpected behavior of the oscillator, especially where the application also uses Port E.7 as GPIO following reset.

As this is an input with a pull-up device during reset, if the pin is left floating the default configuration is for a Colpitts oscillator circuit on EXTAL and XTAL; however, it is recommended to tie this pin externally in electrically noisy environments.

Port E.6 : MODB and Port E.5: MODA

These are GPIO pins that are also used to select the MCU operating mode on reset.

The states of these pins are latched to the MODA and MODB bits at the rising edge of RESET, to configure the operating mode of the device.

These pins should = 0V at reset to select single chip mode. They have internal pull-downs, active only when reset is low; so, if left floating, the default configuration is for single chip mode; however, it is recommended to tie them externally in electrically noisy environments.

Port E.4 : ECLK

In all modes except normal single chip mode, this pin defaults to ECLK (the bus clock).

The ECLK signal can be useful for debugging (ECLK output can also be enabled in normal single chip mode). Consider adding a test point on this signal, but be aware that it is a relatively high frequency clock line.

CAUTION

Take care when using Port E.4 as a GPIO in single chip mode. The reset default of this pin is as an input in normal single chip mode and to output (with the bus clock on it) in special single chip mode. Special single chip mode is enabled whenever a debug cable is connected and a reset performed.

Port E.1 : $\overline{IRQ}$

PE1 is a general purpose input pin and optional maskable interrupt request input that can provide a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode. By default this interrupt input is active low level sensitive but can be configured in software to falling edge sensitive.

Port E.0 : $\overline{\text{XIRQ}}$

PE0 is a general purpose input pin and optional non-maskable interrupt request input that can provide a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode. This interrupt input is active low level sensitive.

CAUTION

If an application requires STOP mode, this pin must be used with care (whether it is the source of the wake from STOP signal or not). Behavior of the STOP instruction is directly linked to the $\overline{\text{XIRQ}}$ functionality. The X bit in the CPU condition codes register masks the $\overline{\text{XIRQ}}$ interrupt (preventing the interrupt vector from being taken) but it does not prevent the $\overline{\text{XIRQ}}$ pin from waking the MCU from STOP mode. As $\overline{\text{XIRQ}}$ is level sensitive, while this pin is low the MCU will not enter STOP mode.

BKGD / MODC

The BKGD/TAGHI/MODC pin is used as a pseudo open-drain pin for the background debug communication link.

The state of this pin is copied to the MODC bit at the rising edge of $\overline{\text{RESET}}$. This pin controls whether the device enters special mode on release of reset. Internally, it has a permanently enabled weak pull-up, to ensure that it enters normal mode if not connected. This pull-up may not be strong enough to ensure adequate rise times for BDM communication with all development tools. If BDM support is required it is recommended to fit an external pull-up resistor. See BKGD Pull-up Value.

Easy access to the $\overline{\text{RESET}}$, BKGD, 0V and VDD5 signals can facilitate debugging. It is highly recommended to include a standard 6-pin header in all design layouts to support in-system debug and reprogramming; the header need not be populated for production. See Standard Serial Debug Interface Connection.

XFC

To use the PLL, an appropriate filter network should be fitted between the XFC pin and VDDPLL. See HCS12 PLL.

Fitting PLL filter components to all designs, whether they use the PLL or not, can be a good idea where BDM tools capable of high speed programming are being used.

Implementing a Standard Serial Debug Interface for the Background Debug Module (BDM)

The BDM module is a single-wire debug interface supported on HCS12 MCUs. Bidirectional communication is via a single pin on the MCU (the BKGD pin). Typically, a BDM interface cable will connect to four signals: BKGD, $\overline{\text{RESET}}$, VSS, and VDD5.

Standard Serial Debug Interface Connection

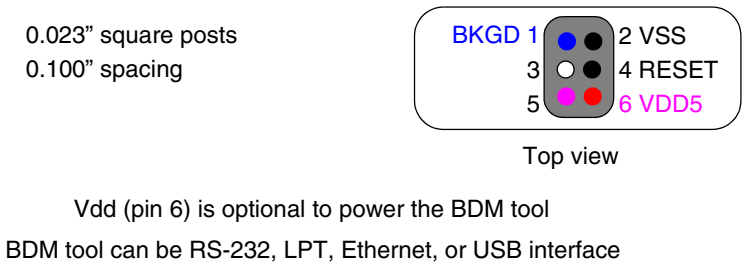


Figure 3. Connector Pinout

Although a debug cable may derive power from a source other than the target board, the target VDD5 and GND signals may be required with some cables to provide a reference level for the cable’s I/O buffers, so routing these supplies to the connector is always recommended.

BKGD Pull-up Value

The MCU BDM module generates ‘speed up’ pulses, so the value of the pull-up is almost irrelevant from the point of view of the MCU, and the specific value of the pull-up required on the BKGD pin is really a debug tool consideration rather than an MCU one.

By default, the BDM module is clocked from the external oscillator clock (EXTAL); however, some BDM programming utilities may select the PLL as the clock source for the BDM.

Aim for t = R*C of about 20% of the maximum BDM speed with the BDM speed = 1/16 of the maximum expected BDM module clock.

So, for a 25 MHz bus => 1 µs bit time => at 100 pF (nominal load) => R = 200 ns / 100 ps = 2 kΩ.

This simplifies to R = 32 x 10^9 / BDM module clock frequency. For example, for 16 MHz, R = 2 kΩ.

Although a low impedance may not be necessary for communication at the application’s target bus speed, using a lower impedance value may be advantageous in electrically noisy environments. However, the resistor value should always be >> ~ 600 Ω, to ensure that a low state will be detected.

The drive capability of the BDM tool used must also be considered — it must be able to drive the selected resistor and line capacitance low. Check any concerns with the BDM cable supplier.

HCS12 PLL

PLL Filter Circuit

The HCS12 PLL allows programmable bus frequencies to be generated from the oscillator clock.

With the PLL disabled:

$$\text{ECLK (bus) freq} = \text{Oscillator (Crystal) Freq} \S 2$$

With the PLL enabled:

$$\text{ECLK (bus) freq} = \text{Oscillator (Crystal) Freq} ¥ \frac{(\text{SYNR} + 1)}{(\text{REFDIV} + 1)}$$

The PLL on the HCS12 requires a three-component passive filter to be connected to the XFC pin, as in Figure 4. The values of the filter components are application specific. The equations for calculating the filter are contained in the device user guide, but it is simpler to use the PLL filter calculator from Freescale.

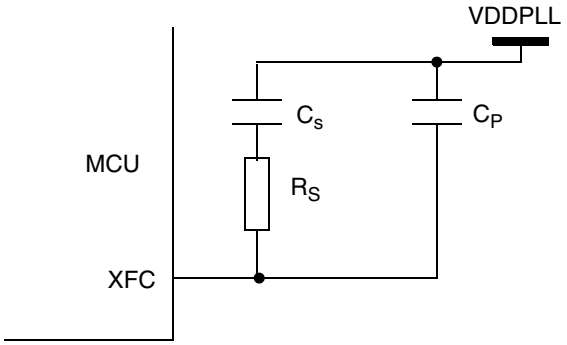


Figure 4. XFC Circuit

If, for some reason, it is decided not to fit a filter network, the XFC pin should be connected via a pull-up resistor (1k to 5k) to VDDPLL.

CAUTION

Never connect XFC to VSSPLL.

If the application does not use the PLL, the software should clear the PLLON bit to disable the PLL following reset.

Oscillator Options

On the HCS12 D-family there are three oscillator options:

- Low power, amplitude controlled Colpitts configuration.
- Full swing (2.5V) Pierce configuration (not available on MC9S12D256x K36N and K79X masks).
- External clock source
  - Uses the same MCU configuration as the Pierce option.
  - The oscillator is a 2.5 V module so an external clock should be ~2.5 V pk-pk.
  - When implementing a clock with a 5V 'canned' oscillator, add a 50% potential divider to reduce the clock to 2.5 V.

On the D-family, a 5 V level on Port E.7 (/XCLKS) at reset will select the Colpitts oscillator option and, as this pin defaults to having an internal pull-up enabled, the Colpitts configuration is the default if this pin is unconnected.

CAUTION

The polarity of this signal can be different on other HCS12 families – check with the individual data sheet.

S12Dx Oscillator Options — Technical Comparison

The following table compares features of the low power, amplitude controlled Colpitts oscillator and the full swing, high drive Pierce oscillator:

Feature	Colpitts	Pierce
Oscillator range	500 kHz–16 MHz	500 kHz–40 MHz
Amplitude control	yes	no
DC-bias cut cap	may be required	not required
Biasing resistor	not required	required
Damping resistor	not required	probably required
Quartz stress	minimal	damping dependent.
EM emission	very low	medium–high
EM susceptibility	medium	low
Current (16 MHz)	170 µA	1100 µA
Current (4 MHz)	100 µA	780 µA
Start time (16 MHz)	1.5 ms	1 ms
Start time (4 MHz)	3 ms	1 ms (no damp.)
Margin (16 Mhz)	300–360 Ω	1.6 kΩ
Margin (4 Mhz)	2–2.5 kΩ	>> 2 kΩ

Start-up time and margin are typical values, measured on carefully laid out PCBs. The current values have been simulated for typical conditions.

The use of a fundamental resonator or crystal is always recommended in preference to an overtone resonator or crystal.

If Colpitts mode is selected, only fundamental mode crystals or resonators may be used.

If Pierce mode is selected, fundamental mode crystals or resonators may be used. Overtone crystals or resonators may be used after careful component selection.

It is recommended that the suitability of a crystal or resonator for use in a particular application be confirmed with the crystal or resonator manufacturer.

The values of the load capacitors are specific to the crystal (and its use with the HCS12 oscillator). Load capacitor values should be confirmed with the crystal or resonator manufacturer.

Common Oscillator layout considerations

Good practice is important when laying out a PCB for any oscillator configuration and it is a good idea to lay out the oscillator first in any design.

The PCB layout is equally as critical when using a ceramic resonator as when using a quartz crystal.

Keep the oscillator components on the same side of the PCB as the MCU and as close to the MCU as possible (allowing for the fan-out of any I/O used on the oscillator side of the MCU).

Keep the oscillator tracks on the same side of the PCB as the oscillator — avoid vias in the oscillator circuit.

Avoid routing other signals on any layers in the region of the oscillator components or tracks. Place an exclusion zone on all layers around the oscillator.

Remove sections of ground or power planes under oscillator components and tracks (to minimize parasitic loading).

Include a 100 nF decoupling capacitor close to the VDDPLL/VSSPLL pins. Avoid vias in the oscillator signal and VxxPLL supply tracks from the decoupling capacitor.

Treat the ground signal for the oscillator as a separate ground, connecting to the main digital ground at one point only, close by VSSR. Where the main digital ground is implemented with a ground plane, it is recommended to keep the oscillator / PLL ground separate from the ground plane.

Routing the oscillator ground via the TEST pin can simplify the layout; this also surrounds the oscillator circuit with a ground ring, which helps to minimize cross-talk and defines an exclusion zone for non-oscillator signals, and reduces the oscillator ground impedance. The TEST pin is a static digital input that will not disturb the oscillator ground.

Keep the adjacent RESET signal clean. Where it is connected off the board or to a long track in a noisy environment, consider adding some series resistance.

Avoid routing signals under the PLL components or tracks, to minimize cross talk.

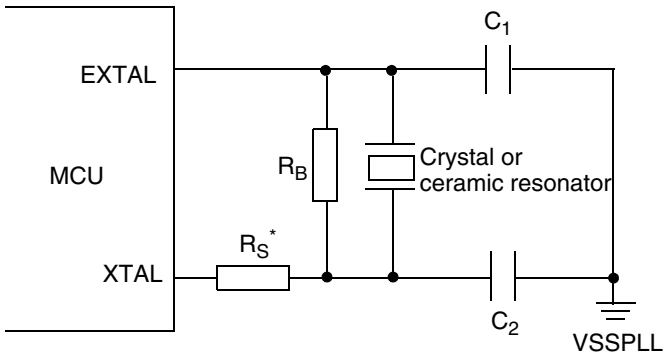
If a PCB is designed to allow both external circuit configurations, it should be optimized for Colpitts mode.

These guidelines are valid for single sided, double sided, and multi-layer boards. On boards with multiple layers, it may be possible to locate the oscillator closer to the MCU by fanning out the adjacent I/O underneath the MCU. Moving the PLL filter components to the back of the board will also help simplify the tracking adjacent to the oscillator.

S12 CRG — Pierce Oscillator

500 kHz to 40 MHz crystal / resonator (not available on MC9S12D256x K36N and K79X masks).

On the D-family, pull $\overline{\text{XCLKS}}$ pin low at reset. This is also the configuration to select for using an external 2.5 V oscillator (square wave).



* R_S can be zero (shorted) when used with higher frequency crystals. Refer to manufacturer's data.

Figure 5. Pierce Oscillator Configuration

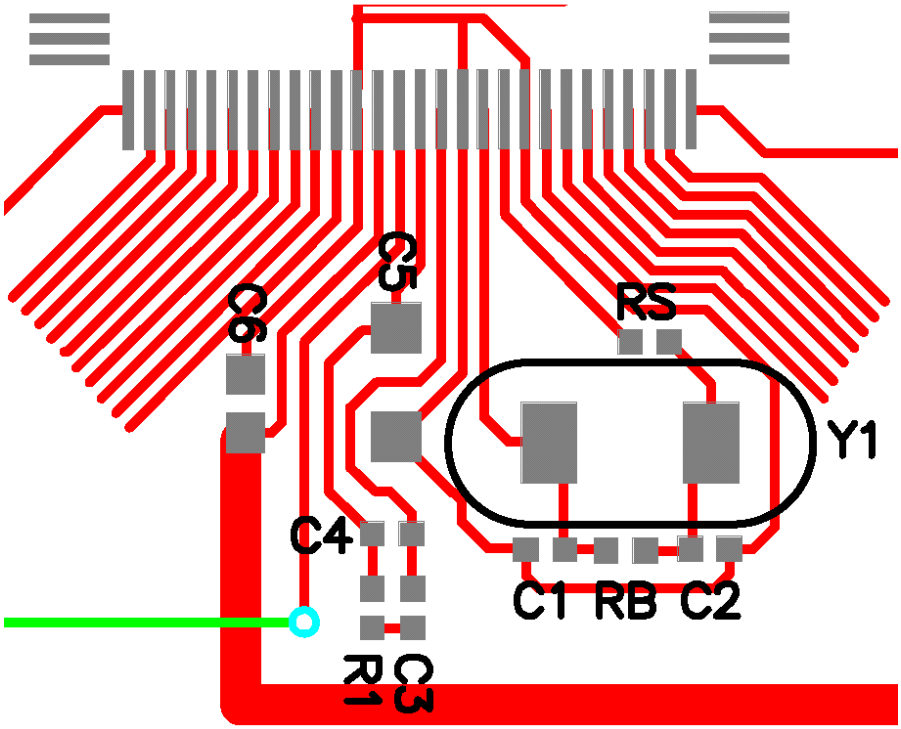
R_B is required to bias the oscillator into its correct operating region. 1 MΩ is a reasonable value for R_B.

Values for R_S, C_1 and C_2 should be confirmed with the crystal or resonator manufacturer.

Additional Pierce Oscillator layout considerations

A key requirement for the Pierce configuration is to minimize the parasitic loading between the EXTAL and XTAL tracks. Keep the EXTAL track as short as possible and tracked away from the XTAL track.

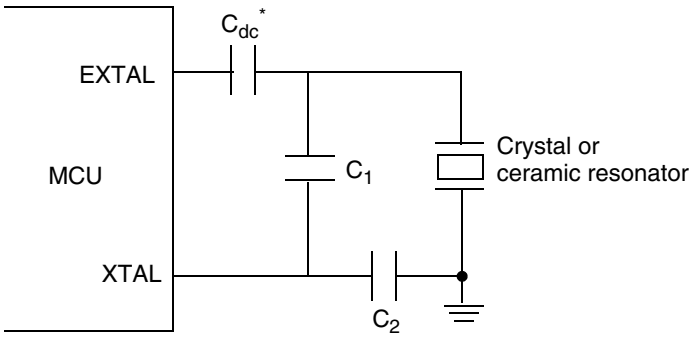
S12 Pierce Oscillator Layout Example



S12 CRG — Colpitts Oscillator

500 kHz to 16 MHz low power oscillator: 1 V pk-pk with DC offset.

On the D-family, pull $\overline{\text{XCLKS}}$ pin high at reset.



* Possible d.c. blocking capacitor (C_{dc}) needed for some vendors' crystals to eliminate 1.1V DC bias. Check with crystal manufacturer.

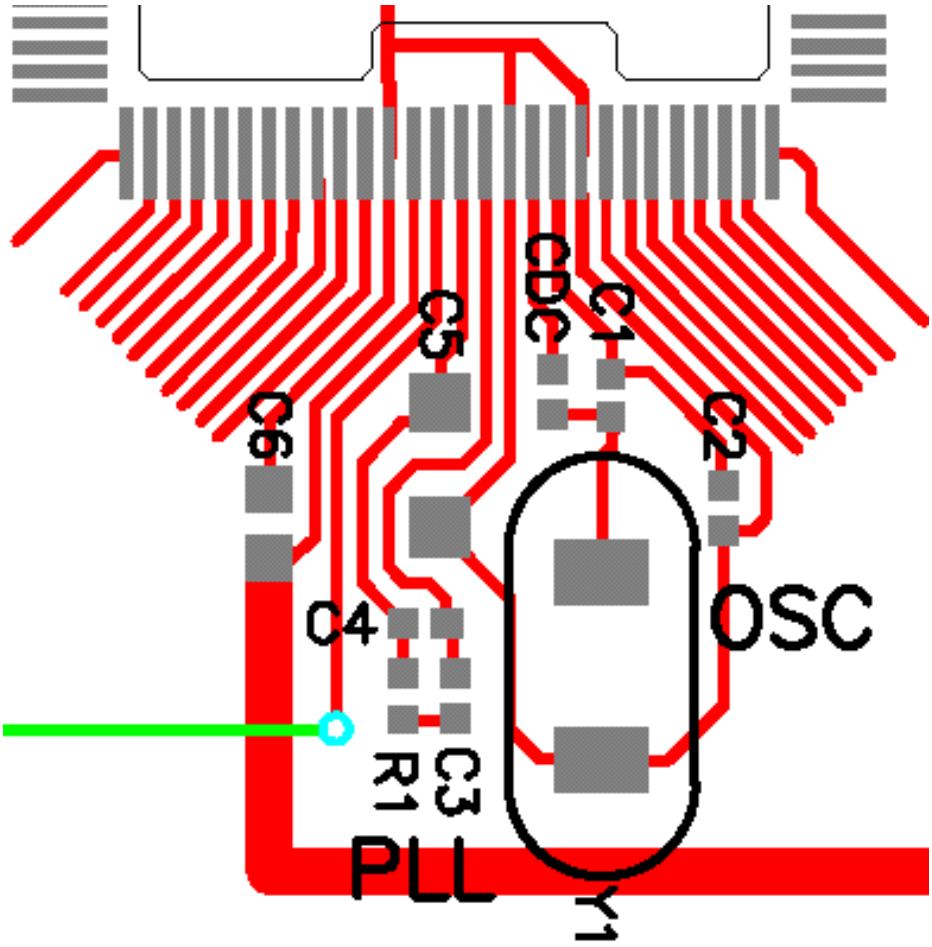
Figure 6. Colpitts Oscillator Configuration

Values for C_{DC}, C_1 and C_2 should be confirmed with the crystal or resonator manufacturer.

Additional Colpitts Oscillator Layout Considerations

A key consideration for the Colpitts configuration is to minimize the parasitic loading of the EXTAL track to ground. Keep the EXTAL track as short as possible and tracked away from other signals, especially ground.

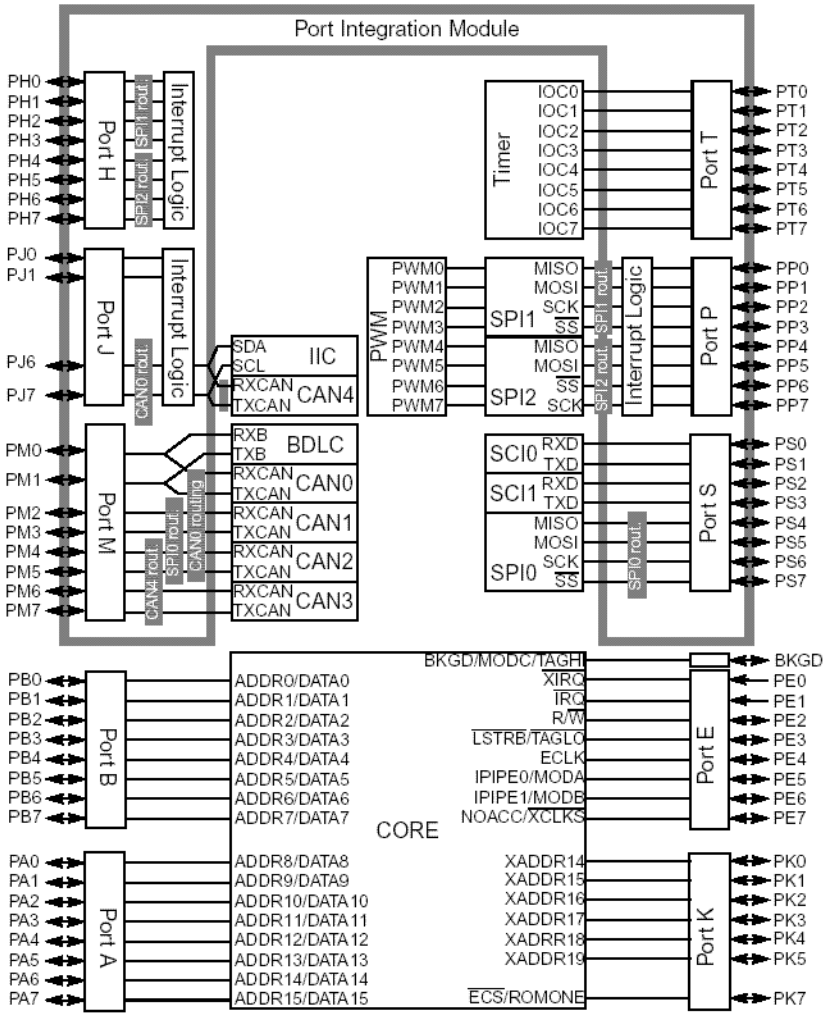
S12 Colpitts Oscillator Layout Example



Pin Considerations — General Purpose I/O

The functionality of each pin is described in the appropriate device user guide. The detailed functionality of the GPIO is described in the appropriate Port Integration Module (PIM) block user guide.

Figure 1-1 is a block diagram of the PIM_9DP256.



HCS12 Core I/O Ports

Ports A, B and K can be used as GPIO. In expanded modes these ports form the expanded address and data bus. Registers for these ports are located in HCS12 core.

Much of Port E can be used for GPIO. In expanded mode, Port E pins support bus control signals. A number of Port E pins have additional control and configuration functions.

XIRQ (Port E.0) supports a level sensitive, non-maskable interrupt vector. It also can wake the device from STOP or WAIT without generating an interrupt vector if the X flag in the CCR is = 1.

IRQ (Port E.1) supports a level-sensitive or falling-edge-sensitive, maskable interrupt vector.

Functions related to Port E are configured in the core Port E Assignment Register (PEAR).

Pull-up control bits for the core I/O ports are in the core Pull-up Control Register (PUCR). Not all pins on Port E have pull devices.

HCS12 Analog Ports

Ports AD0 and AD1 have analog and digital input functionality. Registers for these ports are located in the two 8-channel analog to digital modules, ATD0 and ATD1. An Input Enable Mask Register (ATDxDIEN) allows each digital input buffer to be enabled / disabled on a per pin basis. This means that reading the digital port will not affect pins assigned as analog inputs. There are no internal pull devices available on these ports.

If the ATD module is not enabled, the status of the ATD input stage will depend solely on the status of the ATDxDIENx bits.

- With the ATDxDIENx bit = 0, the digital input stage is disabled. Unconnected input will have no effect.
- With ATDxDIEN = 1, the digital input stage is connected to the pin and an external pull device or drive should be connected.

For electrically noisy environments, it is advisable to connect any unused ATD inputs to ground.

Analog conversion sequences can convert from one to eight channels at a time starting at any one of the channels. An analysis of the ATD sources to be converted may help utilize the flexibility of the ATD control and conversion structure. Sources with similar requirements can then be grouped onto adjacent ATD inputs, and the ATD configured appropriately for each conversion sequence.

The ATD converter's accuracy is limited by the accuracy of the reference potentials. Noise on the reference potentials will result in noise on the digital output data stream; the reference potential lines do not reject reference noise. Ideally the reference supply and ground should be routed separately back the external 5V voltage source.

The reference pins must have a low AC impedance path back to the source. They are practically a static load, and a good bypass capacitor (10 nF or larger) will suffice in most cases. In extreme cases, where high frequency noise is present, series inductors and/or ferrite beads may be necessary, but the ESR should be kept low. Series resistance is undesirable since each enabled ATD module will draw ~ 375 µA from the reference. A potential drop across any series resistance will result in gain and offset errors in the

digital data output stream, unless the reference potential is sensed at the reference input pin and any potential drop compensated for.

Due to the sample-and-hold mechanism of the HCS12 ATD, charge-sharing between the external and the internal capacitances can cause a small voltage drop. Each analog input should have a capacitor, with good high frequency characteristics, between the input pin and V_{SSA}. The size of the external source capacitance will be application dependent; a basic guideline for minimizing the effect of this charge sharing is to keep the external capacitor greater than C_f as defined in the Electrical Characteristics section of the specific device user guide.

- For a maximum 10-bit sampling error of the input voltage ≤ 1 LSB, the external filter capacitor (C_f) should be ≥ 1024 * (C_{INS}-C_{INN}) or ≥ 12 nF.
- For an 8-bit conversion, 1 LSB is four times larger, so the minimum source capacitance for ≤ 1 LSB error is 256 * (C_{INS}-C_{INN}) or ≥ 3 nF.

The source impedance of the signal driver must also be considered when choosing the capacitor size. Optimizing the source impedance may be a compromise:

- External source impedance combined with the input capacitor will create a low-pass anti-aliasing filter, which can be used to attenuate unwanted frequency components and noise. Higher source impedance can result in rolling off of higher frequency components of interest in the input signals.
- Higher source impedance reduces current injection when the input exceeds the rail voltages.
- Lower source impedance avoids and reduces the error generated by input leakage (I_{in}). The maximum external source impedance of an analog signal is limited by the leakage into the pin.

A basic guideline for minimizing the effect of input leakage is as described in the data sheets. When VREF = VRH-VRL = 5.12 V, one 8-bit count = 20 mV and one 10-bit count = 5 mV

- For a maximum 10-bit error of < 1/2 LSB, R_S should be ≤ 2.5 kΩ (= 2.5 mV / 1 µA)
- For a maximum 8-bit error of < 1/2 LSB, R_S should be ≤ 10 kΩ (= 10mV / 1 µA)

See Application Note AN2429 for further details and considerations on interfacing to the ATD ports.

Port Integration Module (PIM) GPIO Ports

Ports H, J, P, M, and S support hardware interrupt functionality and alternative peripheral functionality. Registers for these ports are located in the Port Integration Module (PIM). The PIM automatically switches control of each I/O as appropriate when a peripheral function is enabled for a specific pin.

Each PIM port pin can be configured on a pin-by-pin basis for:

- I/P or O/P function.
- Internal pull-up / pull-down. Approximately 100 µA load when driven by an external source
- Full or reduced drive strength. Useful for controlling EMC on SPI lines and PWM, for example.

Ports H, J and P can also be configured on a pin-by-pin basis for:

- Edge sensitive interrupt inputs with glitch filtering. These can be used to wake the device from low power modes.

A useful feature of the PIM is that when an interrupt is enabled on one of the ports the appropriate pull device for the selected edge polarity is enabled:

- falling edge = pull-up enabled
- rising edge = pull-down enabled

Ports M and S can also be configured on a pin-by-pin basis for

- Open drain for wired-or connections. Useful for connecting multiple communications peripherals to the same bus.

All GP I/O pins default to input on assertion of reset. Some are high impedance with no pull devices enabled, and some have pull-ups enabled. This is reflected in the default value of the associated Data Direction Registers (xDDR).

To achieve minimum STOP / WAIT IDD, internal I/O pull devices should be configured by the application software so as not to conflict with external pin loads.

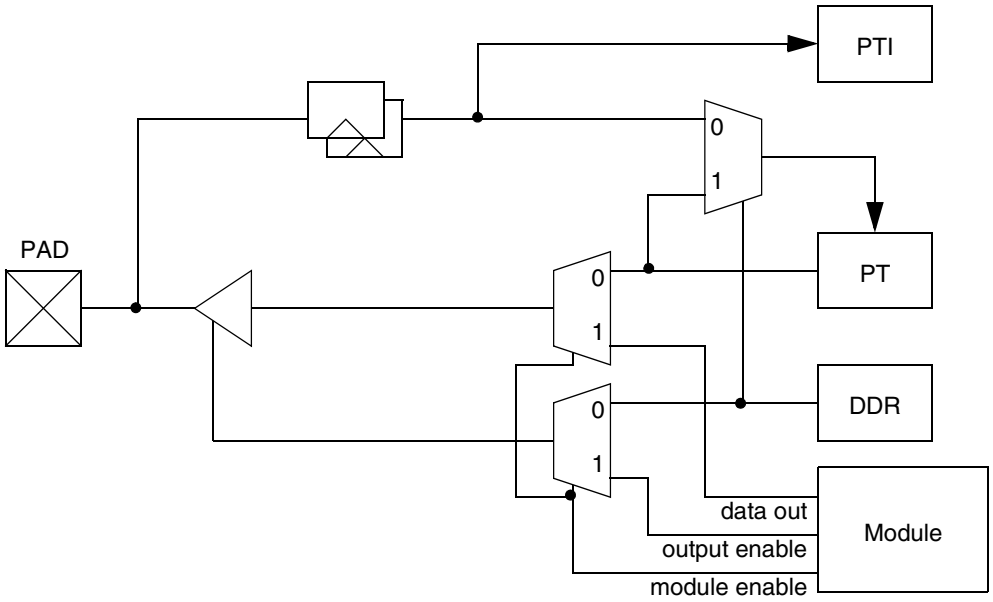
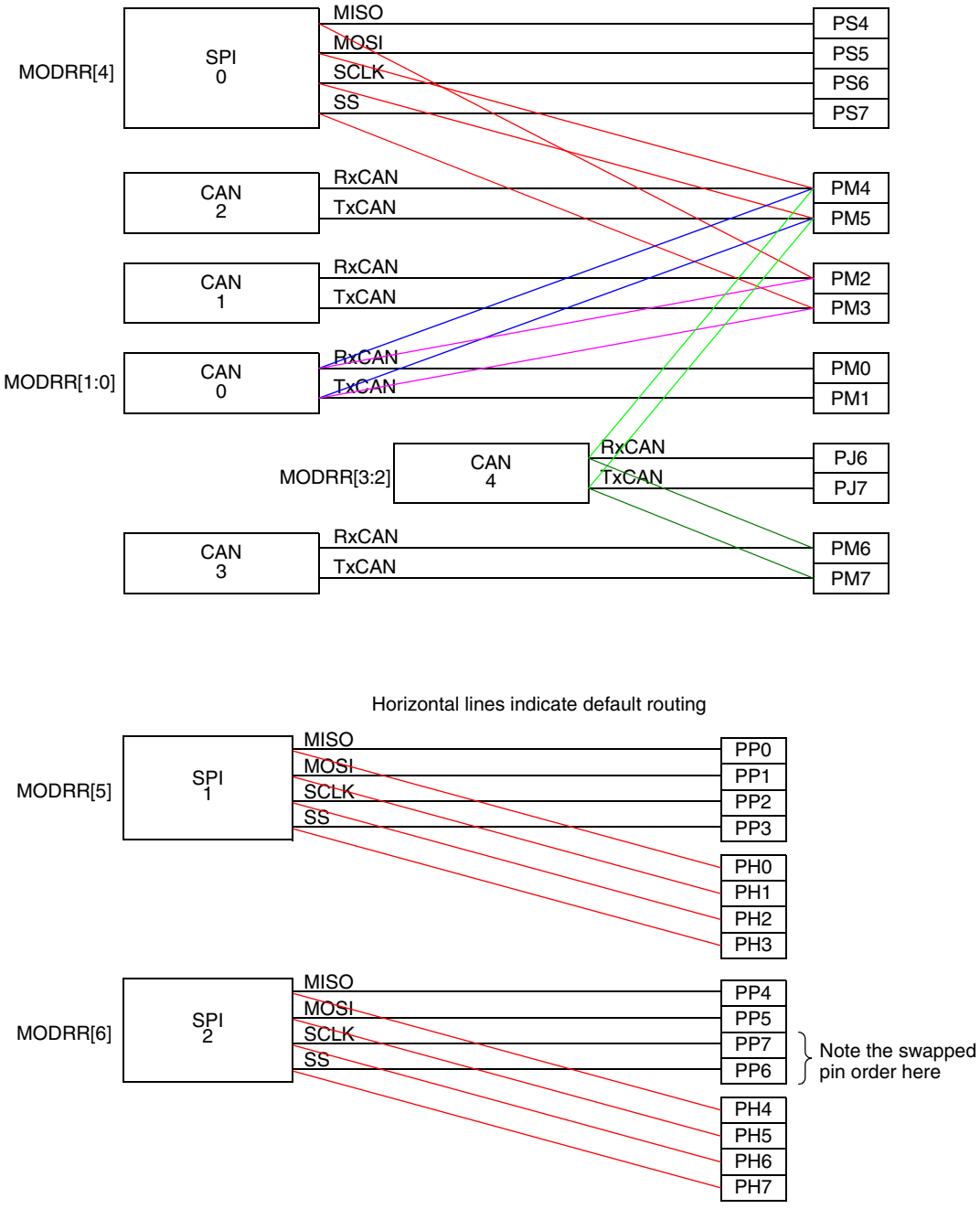


Figure 7. Illustration of Typical PIM GPIO Pin Functionality

MC9S12DP256 MODRR Routing options

The PIM module on the D-family can re-route the I/O connectivity for a number of communications peripherals depending on the value contained in the Module Routing Register (MODRR). This is primarily intended to allow increased peripheral flexibility when using the 80-pin package, but can be used with the 112-pin package to optimize PCB layout.



Managing Unused Pins

If a general purpose input does not have a pull device enabled or is not driven externally, as the input approaches mid-rail (i.e. ~ 2.5 V), a ‘cross-over current’ of ~ 2.5 mA can flow in the I/O stage. This ‘crossover current’ is on a the main I/O drive supply. This is not a concern for the device itself but can directly impact the power supply demand and low power mode currents.

ATD inputs have a slightly different input stage and can be left open-circuit, although it is preferable to ground unused analog inputs to minimize pick-up of unwanted noise.

CAUTION

Leaving unused GPIO undefined is a common cause of unexpectedly high levels of STOP or WAIT IDD. This is not always obvious on every device or assembled module as this is dependent on small variations in the manufacturing process, operating temperature and voltage. Consequently, this is often not detected during development or qualification, but shows up in the application production test or in use where a greater number and range of operating conditions is encountered.

NOTE

HCS12 devices are often available in different packages (mostly 112-pin LQFP and 80-pin QFP). When using a lower pin count variant, it is important to be aware that the I/O available on the largest pin count device is still present but unbonded and must be configured for low power modes. Either enable the internal pull devices or configure as outputs.

There are two approaches to managing unused GPIO: configuring them as inputs, and configuring them as outputs; a combination of the two may be appropriate. In the event of code runaway, a GPIO port could be reconfigured unintentionally; protective software can reduce the impact of this, for either configuration.

Unused GPIO Configured as Outputs

This is a good solution as the pins will have a low impedance to rail. To minimize the impact of the ports being accidentally reconfigured as inputs, enable the internal pull-down resistors (these will only be active when configured as inputs).

Unused GPIO Configured as Inputs

Tie unused inputs to the supply rails, preferably with pull devices. (Where there is no internal pull device, an external pull device will be required.). In some cases, it may be an application requirement for unused inputs to be defined during reset; in this case, all unused pins that default to high impedance must be pulled externally to a supply rail.

Several optional strategies for tying input pins are discussed below. Consideration should be given to the the possibility of I/O conflict occurring, if unused input ports are reconfigured unintentionally as outputs, where:

- two ports are connected together and might be driven with opposing polarities,

or

- a port is connected directly to a supply rail and might be driven to the opposite polarity from the supply rail.

In either case, the maximum IDD specification for the pin will be exceeded, and the MCU will be damaged.

To minimize the impact of the ports being reconfigured accidentally as outputs, configure for reduced drive output, and ensure that the port data registers match the polarity of the pull device(s) / supply rail connection.

There are several possible strategies:

1. Minimum risk, highest cost: pull each unused input pin to a supply rail with an individual pull resistor. This ensures no possibility of I/O conflict, as described above.
2. Highest risk, lowest cost: tie each unused input pin directly to a supply rail. This offers the highest risk of unintentional conflict with a supply rail.
3. High risk, low cost: common up all unused inputs to a single pull resistor to a supply rail. This offers the highest risk of unintentional conflict with another I/O pin.
4. Medium risk, medium cost: a better compromise of cost versus risk is to connect all unused inputs on each I/O port together and connect them to a separate pull resistor per I/O port.

NOTE

Some external peripherals tristate their outputs when disabled (including SPI interface lines). Where this is the case, Stop and Wait IDD can be minimized by enabling the internal pull devices on appropriate inputs while the external peripheral is disabled.

Output Drive Currents

The D-family has an "Instantaneous Maximum current single pin limit for all digital I/O" of $\pm$ 25 mA. If the current on a pin exceeds 25 mA peak at any time, the I/O structure may become may become damaged or suffer degradation. It is strongly recommended to stay well below the 25 mA limit, to avoid peaks exceeding this limit during switching.

The device maximum I/O current is limited by its power dissipation and will be application dependent. The $P_{IO} = \Sigma R_{DSON} \times I_{IO}^2$ term in the data sheet power dissipation calculation indicates the heating effect of the I/O current. Ensure that the total I/O power dissipation plus the internal device dissipation combined does not cause the device junction temperature to exceed the appropriate limit (for C, V or M specification) in the application environment.

In production, I/O limits are tested by holding each pin at the VOL and VOH limit and measuring that the I/O current exceeds the IOL and IOH spec limits respectively (actually a measure of RDSON).

From the VOHL specification it can be seen that in the conduction range the I/O driver has a maximum R_{DSON} = 0.8 V / 10 mA = 80 Ω (at the maximum temperature specified for the device). Typically, RDSON will be lower than this; it will also be reduced at lower temperatures.

When driving high impedance loads such as logic devices the voltage dropped across the output RDSON will be low, and the VOH and VOL levels will be much closer to the appropriate supply rail voltages.

I/O Injection Currents

All digital I/O pins are internally connected to VSSX/VDDX, VSSR/VDDR, or VSSA/VDDA via protection diodes. Taking an input pin above VDD5 or below VSS by greater than a diode drop will cause current to flow to or from the internal device supply rails, via the protection diodes. This is known as “current injection” and is valid as long as the application limits the injected current to within specified limits.

Continuous (IICS)

Up to $\pm$ 2.5 mA per pin. MCU functionality is not guaranteed if any single pin exceeds this value.

Device Total (IICP)

The sum of the injected currents on all pins = $\Sigma \left| \text{IICP} \right|$. Maximum = 25 mA.

Instantaneous Maximum (ID, IDL)

Short duration injection current maximum $\pm$ 25 mA (on any single pin). MCU functionality is not guaranteed but the device will not be damaged. The IICP limit must be respected.

Keep current injection on any individual input less than IICS (2.5 mA) and the total device current injection less than IICP (25 mA). If any pin transient exceeds IICS, MCU functionality is not be guaranteed but, as long as the individual pin current and the total device current remains less than 25 mA, the device will not be damaged.

NOTE

The power supply must maintain regulation within operating VDD or VDDX range during instantaneous and operating maximum current conditions. If positive injection current (Vin > VDD or Vin > VDDX) is greater than IDD or IDDX, the injection current may flow out of VDD/VDDX and could result in external power supply going out of regulation. Make sure that the external VDD/VDDX load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: when no system clock is present, as in STOP mode; when the clock rate is very low, which would reduce overall power consumption.

Analog Input Considerations

In addition to the above constraints, current injection on ATD inputs may cause additional error in conversions of adjacent pins. A portion of the injected current will also be picked up by the adjacent

channels (coupling ratio K), generating an error voltage proportional to the source resistance of the input being converted.

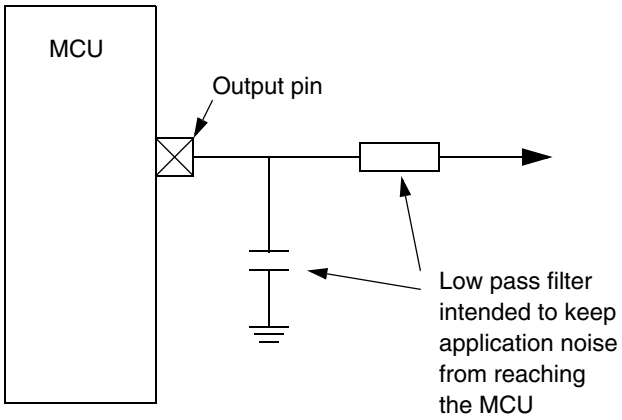
The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

There are two coupling ratios specified:

- $Kp = 10^{-4}$ for positive current injection, where the input is taken above VDDA
- $Kn = 10^{-2}$ for negative current injection, where the input is taken below VSSA.

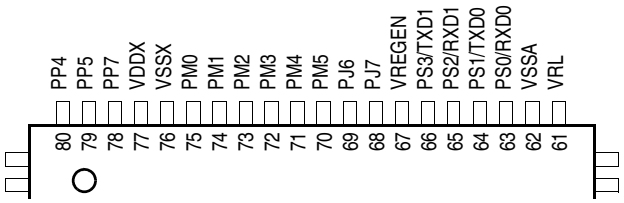
Connecting Capacitors Directly to Output Pins

1. Avoid connecting capacitors directly to output pins as in Figure X in an attempt to prevent system noise reaching the MCU pin.
   The capacitor will appear as low impedance to transitions of the output, resulting in fast rising pulses of current and EMC noise.
   A simple solution is to add some series resistance to the MCU side of the filter. This will increase the rise time of the signal on the capacitor (due to the time constant of the increased effective O/P impedance and the filter capacitor) and reduce the EMC generated.
2. Connecting a large capacitor directly to an output pin (to create a long time delay, for example) can result in exceeding the max IDD spec for the pin and damage to the MCU. Ensure that there is enough series resistance from the MCU to any capacitor to limit the peak current to << 25 mA.

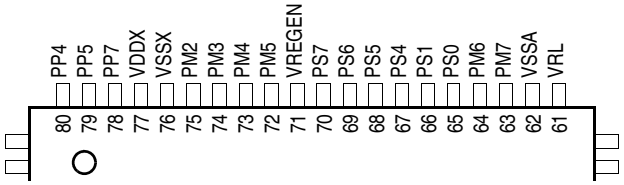


80-Pin Package Considerations

The DB128 80QFP pinout differs from all other 80-pin variants.



Pin Out All D-Family Members except DB128



Pin Out 9S12DB128 in 80 Pin

With the exception of the D32, the 80-pin variant uses the same die as the 112-pin variant. This is not a direct consideration at the hardware design stage as such; however, the application software must configure undefined inputs on port lines that are not bonded out on the 80-pin device, to avoid unexpected I/O IDD. Details of this can be found in the “80-pin Package Pitfalls” section at the end of Engineering Bulletin EB386.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

AN2727
Rev. 0, 12/2004

freescale™
semiconductor