Input/Output (I/O) Pin Drivers on HCS12 Family MCUs

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Introduction

Most microcontroller units (MCUs) must connect to other devices. The input/output (I/O) pins provide this connection. I/O pins are driven by pad drivers which must provide for logic level translation, protection against potentially damaging static charges, and amplification of the internal signals to provide sufficient current drive to be useful outside the integrated circuit.

Generally, microcontrollers interface with high-impedance and well-behaved loads such as other logic circuits. However, users often consider driving other devices such as light-emitting diodes (LEDs) and printed circuit board (PCB) relays.

This application note:

- Examines the behavior of the I/O pins when low-impedance or poorly-behaved devices are driven
- Describes the typical I/O pin driver capability in terms of output voltage versus current for full drive, reduced drive, and with pullup/pulldown devices enabled or disabled
- Provides some background and insight into the pin drivers and related structures
- Provides a process for evaluating source and sink currents
- Interprets the data of the evaluation in a graphic comparison to factory specifications

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Pin Logic Structure

The logic structure for a general-purpose input/output (GPIO) pin is illustrated in Figure 1. The structure includes:

- Output driver
- Input buffer
- Pullup and pulldown sources
- Electrostatic discharge (ESD) protection
- Input hysteresis
- Level shifter
- Control logic

> **NOTE**
>
> *Note that the pulldown structure is generally not present on the core register pins — the 9S12H Family is an exception. The level shifter provides 2.5-V to 5.0-V level translation. The ESD protection will be discussed briefly in ESD Structures. The control logic is used by the MCU to enable and control the various pin modes.*
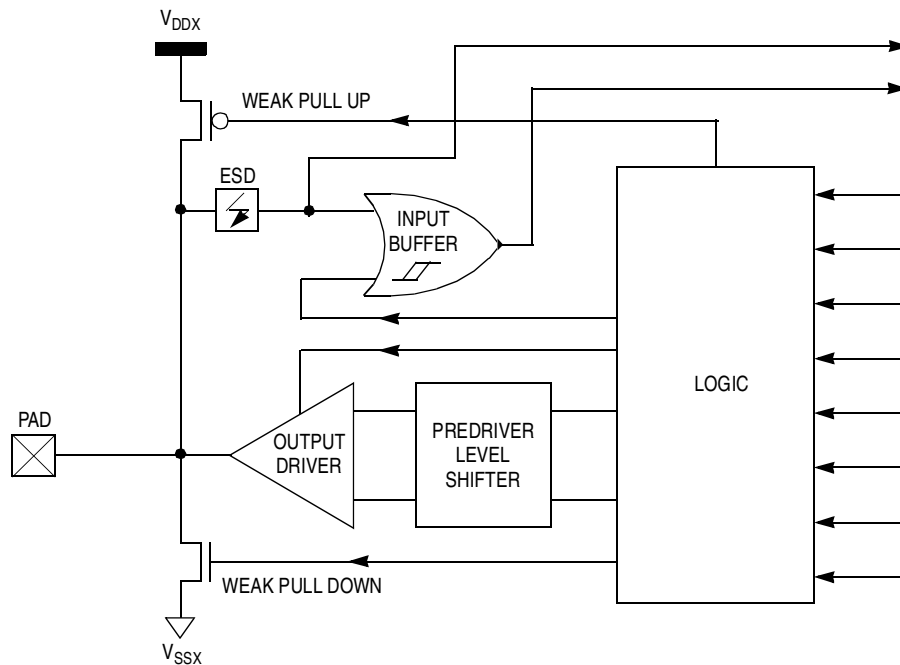
Figure 1. Logic Structure for a GPIO Pin

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The simplified illustration of an output driver in Figure 2 includes two FETs (field effect transistors) that provide a current path between the output pin and both V_{DD} and V_{SS} (or ground). To drive the pin high, the p-channel FET is enabled. To drive the pin low, the n-channel FET is enabled. There is also a series resistor in the output path. The effects of the FETs and the output resistance can be seen in the graphs shown in Figure 11, Figure 12, Figure 8, and Figure 10. Notice the non-linear increase in voltage drop as the current increases. The non-linear portion is due to the FET transfer function.
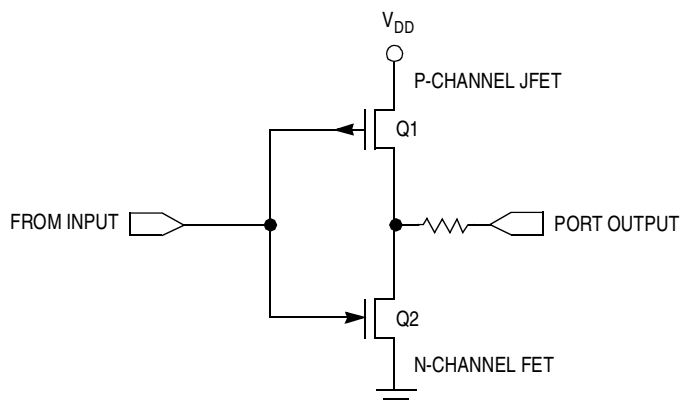
Figure 2. CMOS Output Stage

Pin Types

I/O pins are commonly grouped into 8-bit ports. In some cases there are fewer than eight bits available on the pads for a given port. This generally is a result of pin-count limitations on the device package. Smaller pin-count derivatives give up portions of several ports in order to fit in the smaller package, while retaining as many of the higher-level peripheral functions as possible.

The I/O pins are further divided into those belonging to the processor core and those belonging to the port integration module (PIM). The registers associated with the core and PIM ports are similar in function, but different in layout. The pad drivers for these two port types are also different to accommodate the different functions.

PIM Pins

The PIM is the portion of the MCU that supports the customized peripherals around the processor core. Because the PIM provides the interface between the I/O pins and the non-standard peripherals on the device, it provides a method to control all of the ports beyond ports A, B, E, and K.

Core Pins

Ports A and B are used for expanded mode address and data buses. Port E is used for control signals (including ECLK and bus control). Port K is used for emulation chip select and expanded addressing. All

of the ports associated with the core are available for use as general-purpose input/output (GPIO) in the non-expanded modes.

Because these ports are part of the core, their capabilities are grouped differently than the PIM ports. For example, the core pullups can be turned on or off on a port-wide basis. Pullup/pulldown devices for the PIM can be turned on and off based on an individual bit basis.

NOTE

Some pins have the pulldown disabled or the P-channel field effect transistor (P-FET) disabled, such as the wire OR-ed pins on the inter-integrated circuit (IIC) or serial peripheral interface (SPI) functions. The device user guide for the 9S12DP256B states that the internal structure for all I/O pins, the analog inputs, BKGD, and RESET have identical internal structures. It states further that some of the functionality may be disabled, for example the output drivers, pullup and pulldown resistors are disabled permanently for the analog inputs. (This applies to most of the HCS12 microcontrollers. Two exceptions are the MC9S12E128 and MC9S12C32 Families where the ATD (analog-to-digital converter) pins can be configured as digital outputs as well as digital inputs. See the port integration module (PIM) documentation and the ATD for details.)

Unique Pins

Recent HCS12 MCUs have between 48 and 144 pins consisting of four major types: power/ground, digital, analog, and special function. Special function pins can include oscillator pins, open drain, and super-voltage functions that are enabled by applying a voltage above the normal operating voltage of 5.0 Vdc.

Unused Pins

Unused input pins on the M68HC12 and HCS12 Families of devices should be terminated to ensure proper operation and reliability because these are CMOS devices. CMOS device pins consist primarily of an n-channel and a p-channel field effect transistor (FET). Generally only one of these devices is on at any given time; however, there is a very brief period of time during switching when both devices conduct slightly while one device is turning off and the other is turning on. An un-terminated input can oscillate or float to a mid-supply level, causing both of the FET devices to be in a partial on state, raising device dissipation, increasing noise, and drawing additional supply current.

There are three types of inputs found on most of the M68HC12/HCS12 devices. These are primarily ATD pins, input-only pins, and input/output pins. The best way to terminate input-only pins is to use a pullup or pulldown resistor to tie each unused pin to V_{SS} or V_{DD}. Input-only pins can also be tied together and terminated with a single resistor to V_{DD} or ground; however, it may be more difficult to separate a pin from this connection if an additional input is needed later in the design process.

Unused input pins can also be connected together and then pulled up or down with a common resistor. While use of a common resistor may save component count and cost, it will reduce the flexibility if an

additional input must be made available later in the design process. Pins that may be used as input/output should be terminated individually to permit maximum flexibility if they are needed later in the design process. Pins that are configurable as outputs should never be connected to other such pins, because failure to correctly configure the pins could result in greatly increased power dissipation and may possibly result in damage to the device.

A pin-by-pin review of every MCU design should be performed to ensure that all unused pins are terminated correctly. This should specifically account for package variations where not all signal lines are accessible on pins, such as on reduced pin count packages. These hidden signals must still be treated as unused pins and configured appropriately to reduce power consumption and noise.

Device Damage

Please note that exceeding the device absolute electrical specifications will result in damage to the MCU. The information contained in this application note is provided to show what happens when pins are subjected to loads beyond those in the electrical specification.

Metal migration is caused when the device is heated, even within a small local area, due to excessive current flows. This allows metal atoms to move and causes thinning of traces or shorts to adjacent circuitry within the part. Thinning of traces leads to higher trace resistance, which in turn raises the temperature and continues the process.

Over time, enough metal can be eroded to cause an open circuit or a resistive connection resulting in reduced reliability. Metal layers are designed for a maximum current density, and they have to be operated below those levels to ensure reliability. When the metal and silicon traces are designed, assumptions are made (for example, they are designed for an average current—not peak). A 50% duty cycle is assumed for current driven on a given pad; therefore, average current is assumed to be no higher than 50% of peak current.
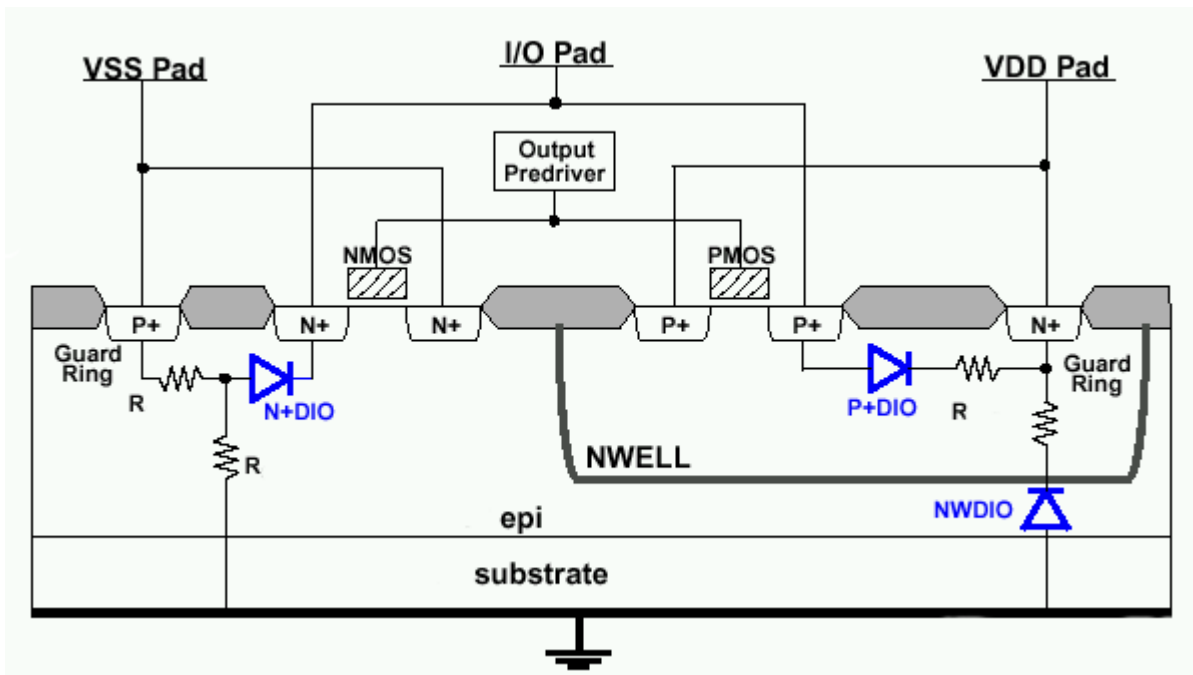
ESD Structures

Figure 3. ESD Structure

The ESD structure generally consists of diodes from the signal pins to the power and ground rail. These diodes are reverse biased with respect to the rails and serve to clamp external voltages to no more than 0.7 V beyond the rails.

NOTE

The following test scenarios were conducted outside of the published device specifications. Do not subject MCUs or their components to unrecommended conditions. Adverse effects may not be immediately apparent, but the damaging phenomena described in this document may deteriorate the life and/or performance of the MCU and/or its components. See the device data sheet or user guide for the approved specifications.

Testing

Testing was completed on the bench at room temperature (25°C) using production samples. A limited number of samples were tested; therefore, the results do not represent the performance of every device.

Injection Current

When the applied voltage or an input pin rises above V_{DD}, current can be injected into the input pin. According to the device electrical specification for the 9S12DP256, injected currents should be limited to ±2.5 mA for any single pin. Injection currents above this specification can cause current to flow in the substrate of the device which can cause increased voltage differential and can affect the accuracy of analog conversions, and in the most extreme case, it can cause damage to the device. A variable power supply was used to raise the voltage applied to an input pin while the internal pullup is disabled. The current flow into the input pin was recorded and is summarized in Figure 4.

Figure 4 shows the effect of a semiconductor diode clamp to V_{DD}.
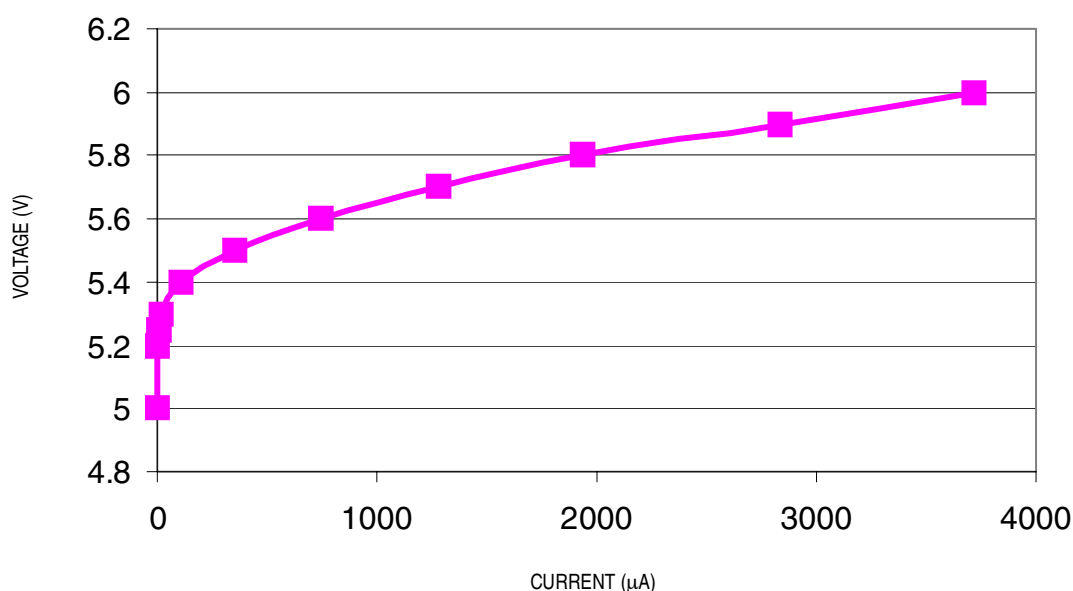
Figure 4. Port A0 — Injection Current versus Voltage
**MC9S12DP256, 25°C, Port A0, V_{DD} = 5 V**

Subjecting a device input pin to current above the maximum limit in the device specification can result in damage to the part. At an injected current of approximately 700 mA, current abruptly drops to 0, indicating an internal failure. (If the input is current-limited, the voltage into the current-limiting resistor can be raised above 11 V without a failure.) The failure is caused by an electrical over-stress (EOS) or by melting of the bond wire which connects the I/O pin to the internal silicon die. EOS can cause the bond wire or metal traces on the die to fuse open. Failure analysis can determine the actual cause of failure by a microscopic examination.

For more information on the effects of electrical over-stress and electrostatic discharge (ESD) damage, please refer to Appendix A and Appendix B at the end of this application note.

Input Characteristics

Specifying the input levels as 65% and 35% of V_{DD} tells the user that by the time a rising voltage reaches 65% of V_{DD} or above, it will be recognized as a logic-high level. When a voltage falls to 35% of V_{DD} or below, it will be recognized as a logic-low level. Voltages between these levels are generally undefined because it is not possible to predict which logic level the MCU will interpret.

Measuring one sample on the bench showed port A0 changed from 0 to 1 when the voltage exceeded 2.582 V with respect to ground. Port A0 changed from 1 to 0 when the voltage was equal or less than 2.440 V. This shows a small hysteresis of 2.582 – 2.440 = 0.142 V (or 142 mV). This is for one sample at 5.0 Vdc and room temperature of approximately 75°F (or 24°C). See Figure 5.
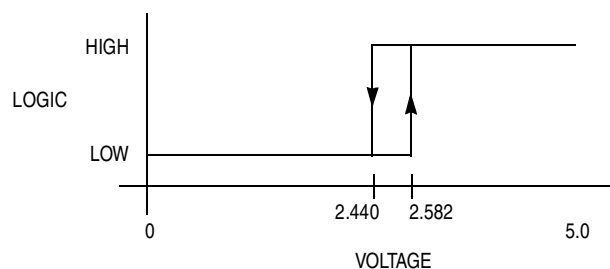
Figure 5. Hysteresis Graph at 25°C, +5.0 Vdc

Note that automated test equipment often measures rise and fall times in terms of percent of V_{DD}. For example, on a common oscilloscope, the rise time is measured as the time a signal takes to move from 10% to 90% or 20% to 80% of V_{DD}. This is not to be confused with the logic recognition levels in the previous paragraph.

Pullups

Pullup resistors help protect high-impedance inputs from oscillation while unconnected and bias pins to an active or inactive state. To ease the integration of an MCU into a user design, pullups are often incorporated into the MCU, itself. The HC(S)12 Families provide internal pull devices. These devices are called pull devices because they can (with some exceptions) be configured to pullup or pulldown. The pull devices are modeled as current sources that can be enabled under user control. In most cases, the user can select whether the pull devices are enabled or disabled. The user can also select the appropriate polarity in some cases.

The device electrical specification states that the pullup and pulldown currents are 10 μA to 130 μA and –10 μA to –130 μA. Some manufacturers list these as impedance (ohms) and others list them as current sources or sinks (μA or mA). In the HCS12 Family, these devices are weak N-channel and P-channel transistors rather than resistors so it would not be appropriate to specify an impedance in ohms.

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Pullup Current

The pullup current was measured by a current meter in series between the input pin and a variable power supply. With the power supply set to 5.0 Vdc, there is a slight leakage current into the input pin. This is caused because there is a small voltage drop between the MCU's power supply and the input pin. At approximately 4.9 Vdc, the current is 0 μA (as expected). As the variable voltage is slowly reduced to 0 V, the current was measured and recorded. Figure 6 summarizes the results. The maximum pullup current observed is approximately 57 μA.

It should be noted that the pullup mechanism is a weak semiconductor device and not a physical resistor so the I-V characteristic is not linear, as would be expected for a pure resistor.
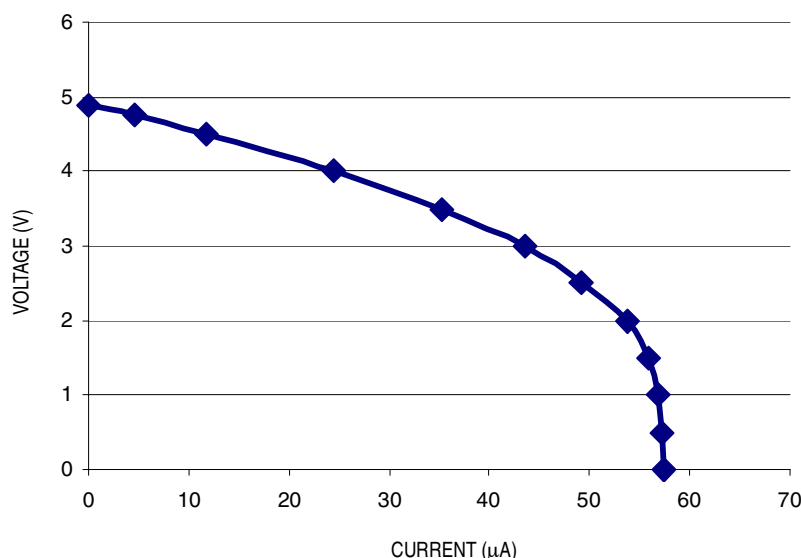
Figure 6. Port A — Pullup Current versus Voltage

Output Characteristics

In Figure 7, Figure 8, and Figure 11, the port A0 pin is driven to a logic 1. In Figure 9, Figure 10, and Figure 12, port A0 pin is driven to a logic 0. When a heavy load (low impedance) is applied, the pin is not capable of forcing the intended level. Freescale Semiconductor specifies a maximum allowed current that will still result in an output voltage that meets the specified limits for a logic 1 or logic 0. On some devices (such as M68HC08 MCUs), different ports may have different source and sink current capability. On the HC(S)12 Families, many ports have similar drive capabilities (with the exception of the motor controller ports on the HC9S12H Family). This application note includes graphs of output voltage versus current for conditions exceeding the specified standard load.

In the manufacturer specification, I/O drivers are characterized by the voltages observed at specified maximum current levels for both the high and low logic levels. The test results for V_{OH} versus source

current are shown in Figure 8 and Figure 11. To simplify the graph, one general-purpose input/output (GPIO) pin is shown. The GPIO pins are contained in two sections of the MCU:

- Core
- Port integration module (PIM)

The core includes ports A, B, E, and K. The port integration module (PIM) includes ports M, P, S, T, H, and J. Data was collected for ports A0, A7, B7, E7, and K5. Plotted data for port A0 is representative of all the port pins based on previous testing.

The graphs also show a dashed vertical line to indicate the maximum current for which the pad drivers were designed. The current and voltage thresholds specified in the device electrical specification are shown for comparison.

The electrical specification section of the device user guide specifies the absolute maximum amount of current source or sink. For example, the 9S12DP256 user guide specifies that the maximum amount of current source or sink allowed for any single I/O pin is ±25 mA. Figure 8 and Figure 10 show that higher currents can be supplied, however V_{OH} and V_{OL} specifications do not apply and damage to the MCU may result. The factory specifications are conservative to ensure that all devices meet the specifications while taking into account normal voltage, temperature, and process variation. Sourcing or sinking more current than the absolute maximum ratings can damage the MCU.

When this document was written, the MC9S12 Family did not specify maximum current for all pins combined. (Limits are implied by device thermal characteristics, which are described in the device user guide or data sheet.) Some other MCUs have both a maximum pin current specified (before V_{OL} and V_{OH} may go out of specification) and a maximum total device current specified (to prevent metal migration).

Source and Sink for Full-Drive Currents

To test the current that an output pin can source, the output pin is tied via a resistor to ground (V_{SS}) (see Figure 7). The resistance is then varied while the voltage (with respect to ground) is held (relatively) constant and the current flowing out of the pin is measured. For this series of tests, the voltage and current are measured with two digital multimeters. The values are recorded and plotted in the following sections. Voltage (the independent variable) is plotted on the Y axis, and current (the dependent variable) is plotted on the X axis in Figure 8 and Figure 11.

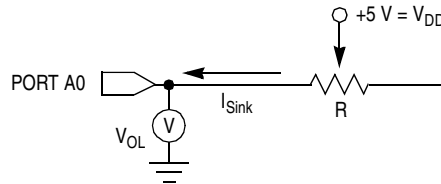**Figure 7. Source Circuit**

Input/Output (I/O) Pin Drivers, Rev. 0
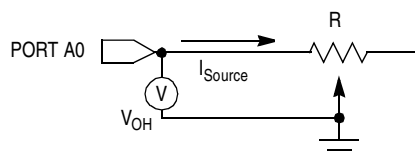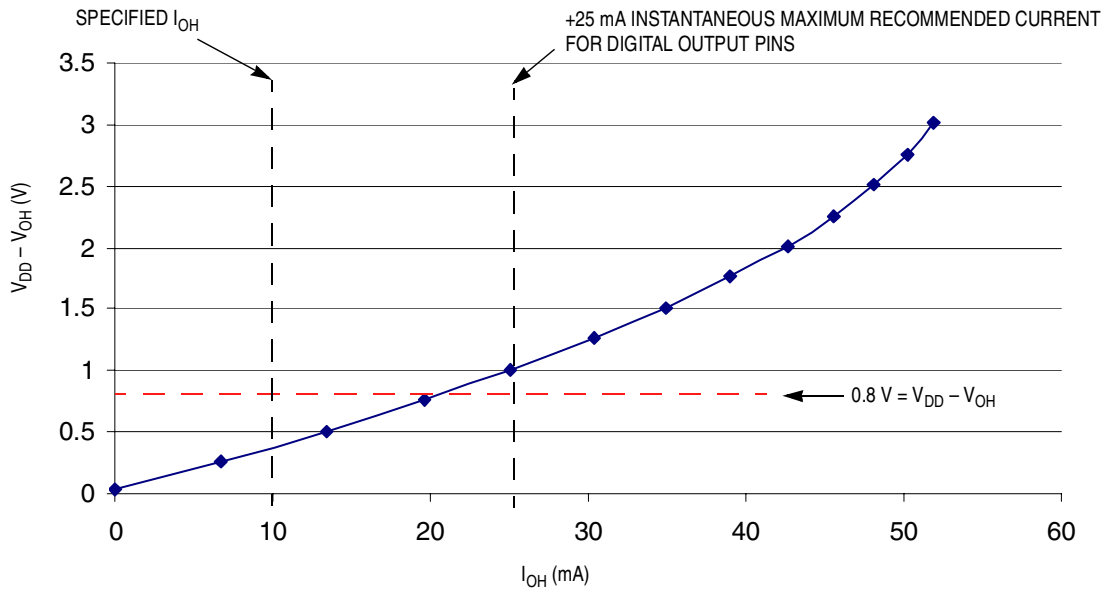
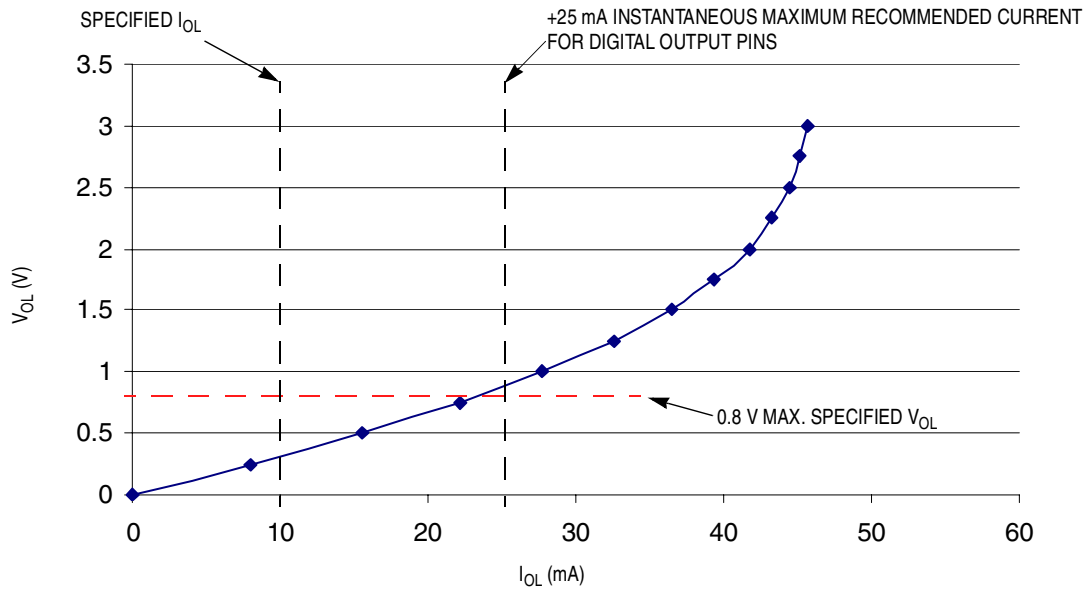**Figure 8. V_{OH} versus Source Current — Full Drive**
MC9S12DP256, 25°C, Port A0, V_{DD} = 5 V

The current that an output pin can sink is measured by connecting the output pin via a resistor to V_{DD} and driving the output pin low (see Figure 9). Again, the resistance is varied and the voltage at the pin and the current through the resistor are measured using two digital multimeters. The values are recorded and plotted in Figure 10 and Figure 12.

Figure 9. Sink Circuit

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SPECIFIED I_{OL}

+25 mA INSTANTANEOUS MAXIMUM RECOMMENDED CURRENT
FOR DIGITAL OUTPUT PINS

0.8 V MAX. SPECIFIED V_{OL}

V_{OL} (V)

I_{OL} (mA)

**Figure 10. V_{OL} versus Sink Current — Full Drive
MC9S12DP256, 25°C, Port A0, V_{DD} = 5 V**

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Source and Sink for Reduced Drive

HCS12 I/O pins include a reduced current mode. This mode is provided to reduce EMI emissions in cases where the load being driven by the I/O pins is light and full drive strength is not needed. The reduced drive strength is approximately one third of full drive strength. Reduced drive strength is configurable on the PIM-based I/O ports through individual reduced drive registers for each port (RDRx). (This would include all I/O ports other than ports A, B, E, and K.)

Figure 11 and Figure 12 show V_{OH} and V_{OL} versus current for the reduced drive configuration of the GPIO pins.
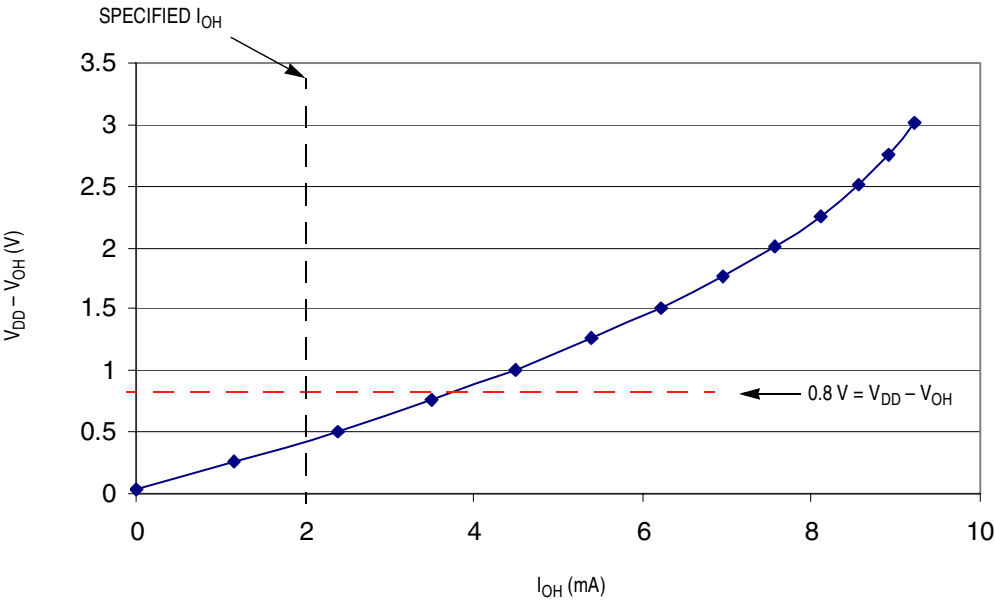
**Figure 11. V_{OH} versus Source Current — Reduced Drive
MC9S12DP256, 25°C, V_{DD} = 5 V**

Input/Output (I/O) Pin Drivers, Rev. 0

Figure 12. V$_{OL}$ versus Sink Current — Reduced Drive
MC9S12DP256, 25°C, V$_{DD}$ = 5 V

Capacitive Loading

Device electrical 7specifications typically show parameters such as V$_{OH}$, V$_{OL}$, I$_{OH}$, and I$_{OL}$ plus absolute maximum electrical signal levels and timing criteria based on a specified loading on the I/O pin (in terms of impedance and capacitance). For the HCS12 Family of MCUs, this capacitive loading is specified as 50 pF (pico-Farads or 10^{-12} Farads).

Signals with low capacitive loading have fast expected transition times. Increased capacitance on a pin will cause the signal to have a longer transition time. The impedance of the internal circuitry restricts the available current that can flow into or out of a pin. To charge or discharge a capacitive load, the current and the capacitance form a time constant that increases with reduced current or increased capacitance.

Device specifications are based on design targets and are validated after testing many parts across temperature, voltage, and a normal range of process variation. This testing is performed on a tester which also puts a capacitive load on the I/O pins. The electrical specification generally includes an input capacitance specification that accounts for pin capacitance.

When bench testing, the capacitance of oscilloscope probes, printed circuit board traces, and parasitic capacitance can increase rise and fall times of signal transitions. One way to determine the maximum transition times is to add a large capacitor between an output pin and ground and determine the effects on signal timing. To minimize the effects of stray impedance, component leads and scope probe leads must be very short (or low-capacitance probes must be used) when measuring timing.

Figure 13 shows an output trace with multiple reflections of the signal transition superimposed on each other. This is the result of poor measurement techniques.

Input/Output (I/O) Pin Drivers, Rev. 0
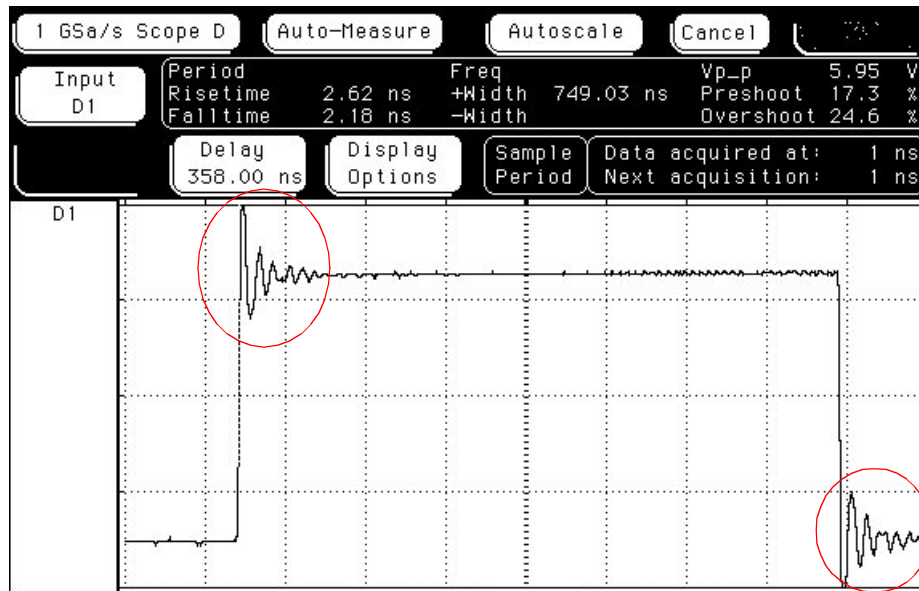
Figure 13. Effect of Long Leads and Stray (or Parasitic) Impedances

By minimizing the length of component leads, PCB traces, and wire used to connect the scope probe, many of these effects can be reduced. Figure 14 shows the effect of capacitive loading at 0 pF, 200 pF, and 470 pF with very short leads. (The capacitor value is that of bulk capacitance added to the I/O pin. The scope probe adds approximately 10 pF to the existing pin capacitance—which is approximately 2 to 3 pF—and any existing PCB parasitics. PCB parasitics are approximately 7 pF on a 4-layer evaluation board.) Minimizing the parasitic or stray component effects makes it clear that the effect of increased capacitive loading results in longer rise and fall times. It now becomes obvious that exceeding the capacitive load for an output pin will result in longer transition times. Adhering to the loading limits in the device electrical specifications will help ensure that the timing specifications can be met in practice.
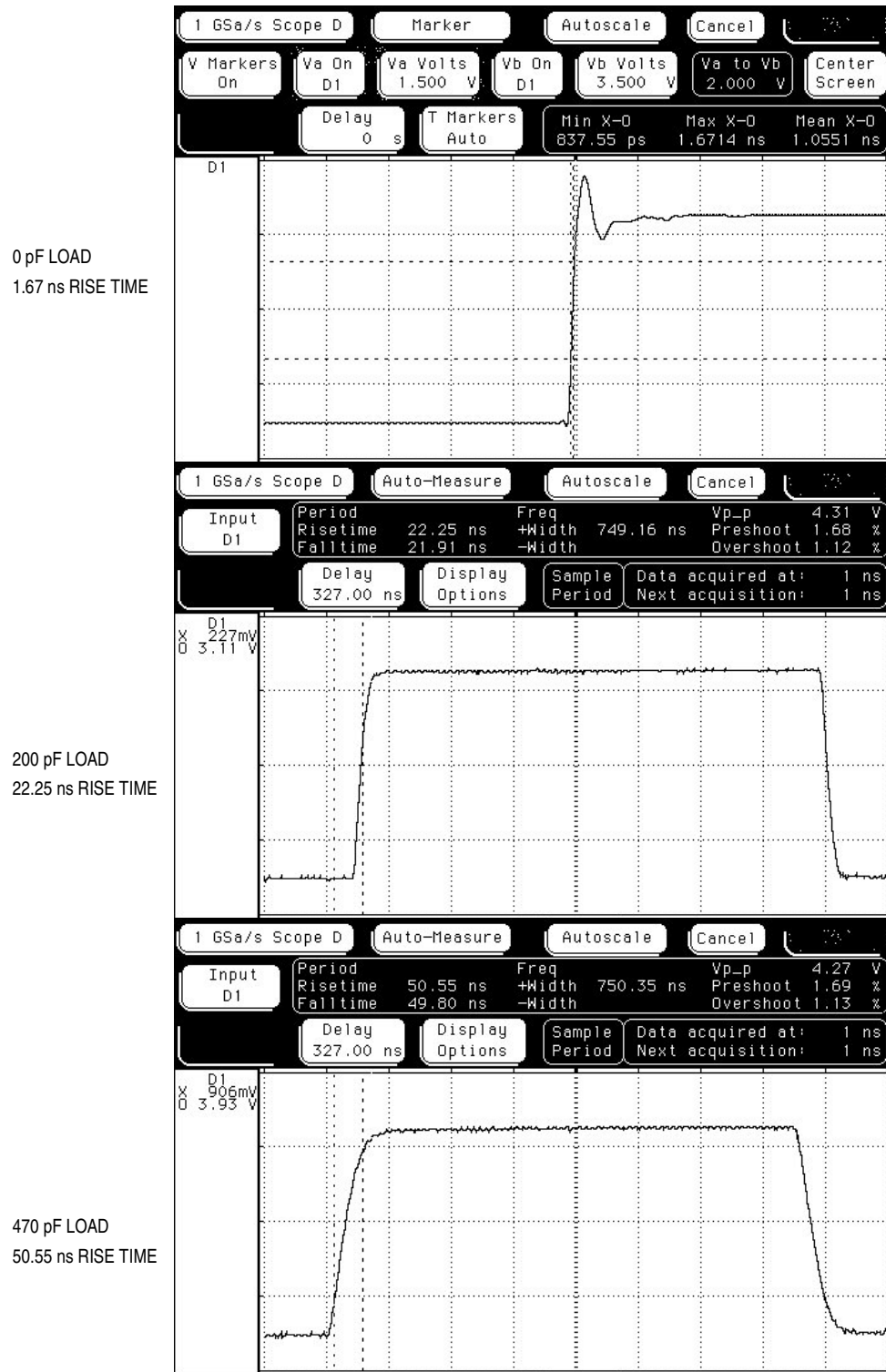
Figure 14. Rise Times under Different Loads
(Rise Times Were Measured from 20% to 80%)

Input/Output (I/O) Pin Drivers, Rev. 0

Inductive Loading

When driving a load such as an inductor or capacitor that might result in voltages beyond V_{DD} or below V_{SS}, one should take care to provide external circuitry (such as Schottky diodes), which will protect both the MCU and the internal ESD diodes. Schottky diodes are suggested because they have a faster switching time and a lower forward voltage (of approximately 300 mV) than the internal ESD diodes (which have a forward voltage of approximately 700 mV). Using external Schottky diodes will ensure the external diodes conduct before the internal diodes thus protecting the MCU from damage as a result of reverse EMF or back EMF (electro-motive force).

The example waveforms (Figure 15 and Figure 16) show the results of driving a 5-V relay with and without an external Schottky diode. The waveform is a square wave which switches between +5 Vdc and 0 Vdc. The falling edge of the waveform shows an overshoot, which is a result of the back EMF being generated when current flowing through the relay coil is interrupted. The coil attempts to preserve the flow of current and in doing so causes a negative voltage to be generated briefly. (The relay coil impedance is 250 Ω and 740 μH.)
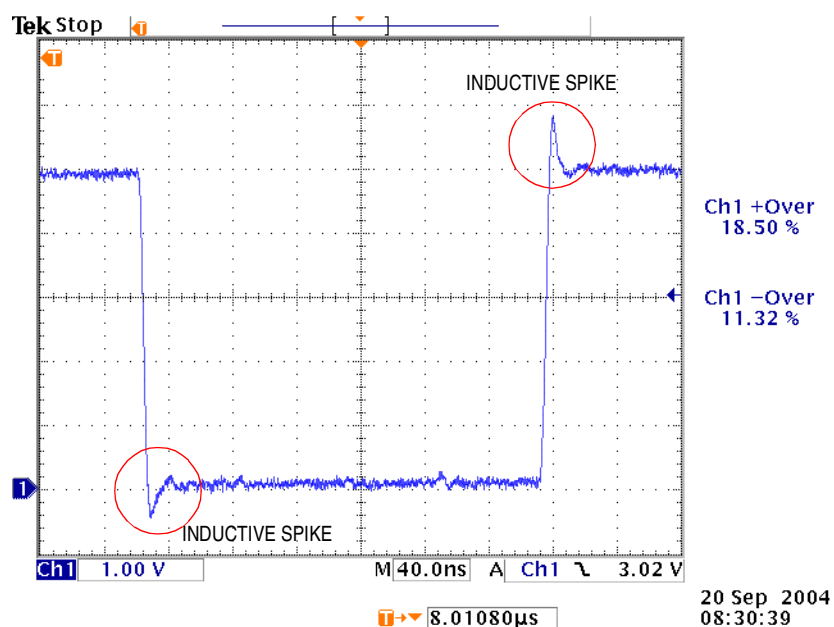
Figure 15. Inductive Spike
Back EMF Clamped by Internal I/O Diodes

The back EMF is clamped in Figure 15 by the ESD protection diode internal to the MCU pin. After applying a reverse-biased Schottky diode from the pin to ground, the effect of reduced back EMF amplitude can be seen in the Figure 16.

Input/Output (I/O) Pin Drivers, Rev. 0
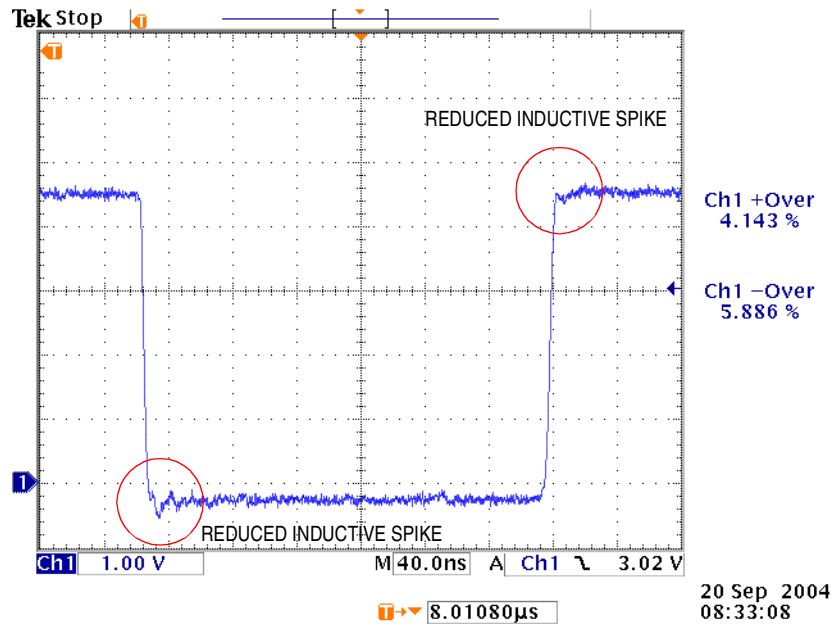
**Figure 16. Reduced Inductive Spike
Back EMF Clamped by External Diodes**

Conclusion

The graphs and data in this application note suggest that MCU GPIO pins can source or sink much more current than the official specification recommends. Though adverse effects may not be immediately apparent, the damaging phenomena described in this document may deteriorate the life and/or performance of the MCUs and/or its components. To improve the life and performance of Freescale Semiconductor MCUs, designs and applications must comply with approved specifications in the device data sheet or user guide.

References

Dabral, Sanjay and Maloney, Timothy. *Basic ESD and I/O Design*. New York: John Wiley and Sons, Inc., 1998.

Also see Appendix A and Appendix B.

Input/Output (I/O) Pin Drivers, Rev. 0

Glossary

ATD — analog-to-digital converter

CMOS — complementary metal oxide semiconductor

EMF — electro-motive force

ESD — electrostatic discharge

FET — field effect transistor

GPIO — general-purpose input/output

Hysteresis — A function which lags or falls behind. Generally a function whose transition in a forward direction is located differently in the reverse direction.

I/O — input/output

MOS — metal oxide semiconductor

PIM — port integration module

V_{OH} — voltage, output high

V_{OL} — voltage, output low

V_{DD} — supply voltage; generally +5 Vdc (historically drain voltage)

Vdc — volts, direct current

V_{SS} — reference voltage; generally +0 Vdc or ground (historically source voltage)

Appendix A

MOTOROLA

Failure Analysis Technical Report on Electrical Overstress (EOS)

What is EOS?[1]

Electrical overstress (EOS) is the misapplication of excessive voltage or current to the external leads of an integrated circuit. The damage caused by EOS is actually a result of the total energy applied to the device. Externally, the damage will result in open, short or leaking pins. It can also affect the devices functionality. Internally, the result is typically seen as fused bond wires or damage to the die metalization.

EOS vs. ESD

The key difference between EOS and electrostatic discharge (ESD) is the rise time of the energy pulse. Rise times associated with an ESD event are in the 5-20 ns range while the rise times for EOS events tend to be much longer. Failure mechanisms associated with both types of events are strictly due to localized heating. Where the localized heating occurs is key understanding the failure mechanisms. Damage seen on bond wires and die metalization are typically associated with EOS (slow rise time, high energy) while junction degradation, poly melt filaments and contact damage are associated with ESD (fast rise time, high energy). Typically, most ESD damage is only visible through deprocessing and SEM inspection. Most EOS damage is visible through an optical microscope.

Typical Failure Modes for EOS

The most common failure modes indicating an EOS event are open pins, shorted pins and leaking pins. Figure 1 shows the curve traces for each of these situations on a standard I/O pin. Open pins are the result of bond wires or die metalization which has been vaporized and has fused open. Shorted and resistive pins are usually due to die metalization and oxide melting then reflowing into adjacent metal. Leaky pins can also be due to the reflowing of metal and oxide in and near active areas.
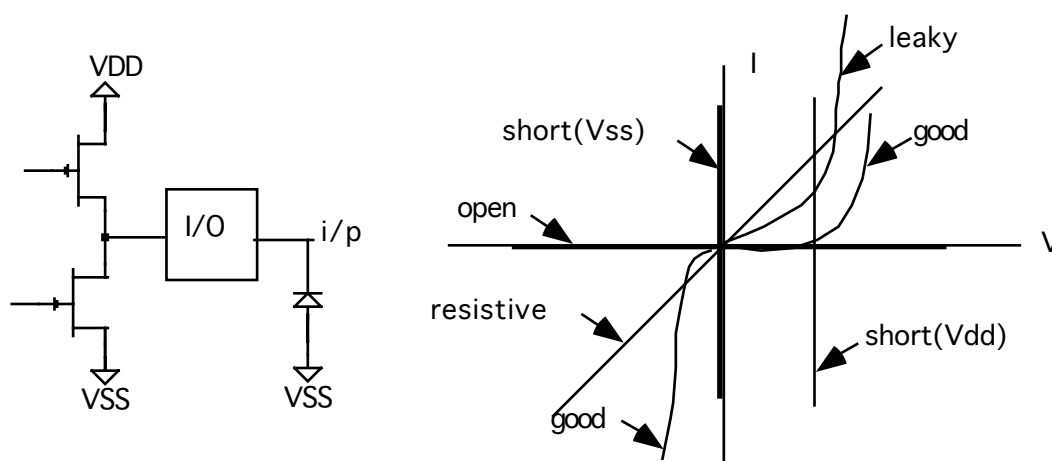

Figure 1. Schematic for a typical I/O pin and the curve traces which could be associated with the pin.

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[1] This technical report was compiled by Carole LeClair of Freescale's CSIC Failure Analysis Lab.

Failure Analysis Technical Report on Electrical Overstress (EOS)

Typical Failure Mechanisms for EOS

The physical failure mechanism which results from an EOS event is greatly dependent on the total energy applied to the pin. Both time and current play roles in determining the total energy. Temperature can also be a factor since it is the act of melting metal and oxide which results in an EOS failure.

There are really only two failure mechanisms normally associated with EOS, fused bond wires and fuse die metalization (Figures 2 and 3). The average bond wire for a device is 1 ml in diameter and approximately 60 mils long. A DC current of 1 Amp would be sufficient to fuse a bond wire of this dimension. Higher current pulses of shorter duration could also fuse a bond wire. For example, a 5 Amp, 1 msec pulse would most likely fuse the average bond wire. In both these cases, the energy dissipated is equivalent to the energy absorbed by the bond wire. Simple calculations show that when the temperature necessary to absorb this energy exceeds the melting temperature of the gold bond wire, the wire will fuse.

The second mechanism associated with and EOS event is fusing of die metalization. Typically, these events are extremely high current spikes of short duration (<170 μsec). In this event, the heat dissipated on the die is conducted way from metalization through the SiO_2 to the substrate. SiO_2 is a fairly good thermal conductor therefore the current needed to fuse the die metalization is fairly high, typically around 10 Amps.

Since heat plays a big part in creating the EOS damage, it is important to note that in plastic encapsulated devices, the actual fused metalization may not be visible due to carbonized plastic residue left on the die. This carbonized plastic is the direct result of the locally absorbed energy and it's resulting high temperature.
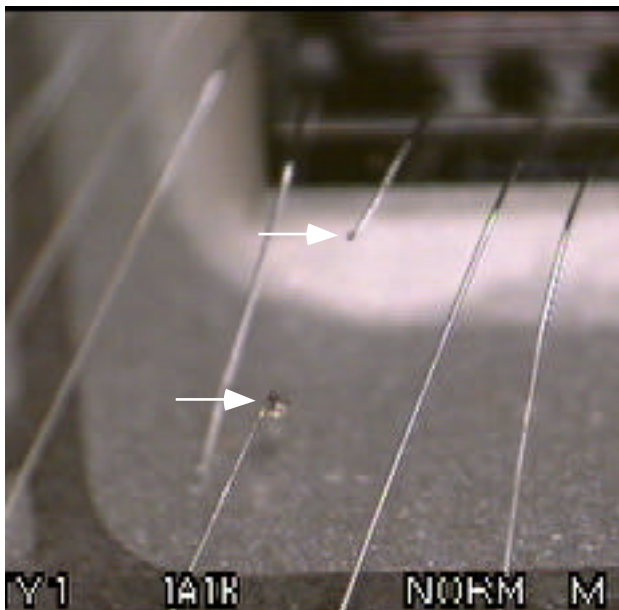

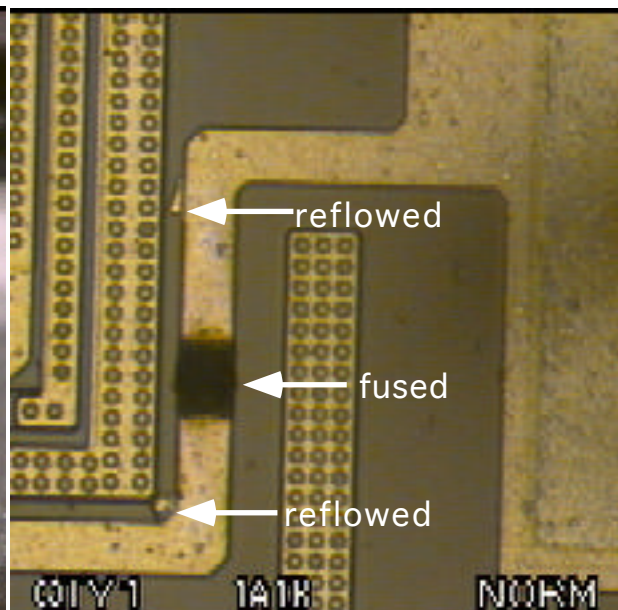**Figure 2.** Optical micrograph of a fused bond wire..

Figure 3. Optical micrograph of typical EOS damage. Both fused and reflowed metal are evident.

Appendix B

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Electrostatic Discharge (ESD) in Integrated Circuits - A Primer   (rev 2.0 - 5/5/95)

What is ESD?

Electrostatic Discharge is the application of a short duration high energy pulse to the external leads of an integrated circuit. ESD is often confused with Electrical Overstress (EOS). While both ESD and EOS failures are the direct result of localized heating, the location of the damage differs. Damage seen on bond wires and die metallization are typically associated with EOS, while junction degradation, contact damage and gate oxide breaches are more often linked with ESD events. The reason for this difference in failure mechanisms is the rise time and duration of the energy pulse. While ESD events may only take less than a microsecond to happen, EOS events are much slower to occur, and typically last much longer.

An electrostatic discharge happens when two objects at different potentials come in contact with one another. Charge is transferred from one body to the other until they are both at the same potential. The time required for this charge transfer to take place can vary, and depends on the characteristics of the charged bodies, such as their capacitance and the resistance of the discharge path between them. This charge transfer is referred to as an ESD event.

How can objects charge up?

Objects charge in a number of ways. Perhaps the most common is through frictional charging, also known as triboelectric charging. This involves the transfer of electrons from one object to another through direct contact. Several factors can affect the efficiency of the charge separation, such as relative humidity. For example, walking across a carpet in summertime when it's humid will not generate much charge, but in wintertime, when the relative humidity is low, a substantial charge can be built up, only to be discharged via an ESD event when you touch a lamp or doorknob. Objects can also charge up by being inside a strong electric field. The components in your television are in close proximity to the electric field generated by the picture tube. When the TV is switched off, there is a great deal of static electricity on the screen and case. Cracking and popping is also heard. This is the discharge of the field induced charge that has built up on the various components inside the TV.

How are   IC characterized with respect to ESD susceptibility?

In order to characterize devices, it is necessary to subject them to stresses that are repeatable and predictable. This has resulted in the development of three ESD models used to approximate real world ESD events. The first two deal with a charged body discharging to or through an IC to ground, while the third simulates a charged IC discharging to ground.
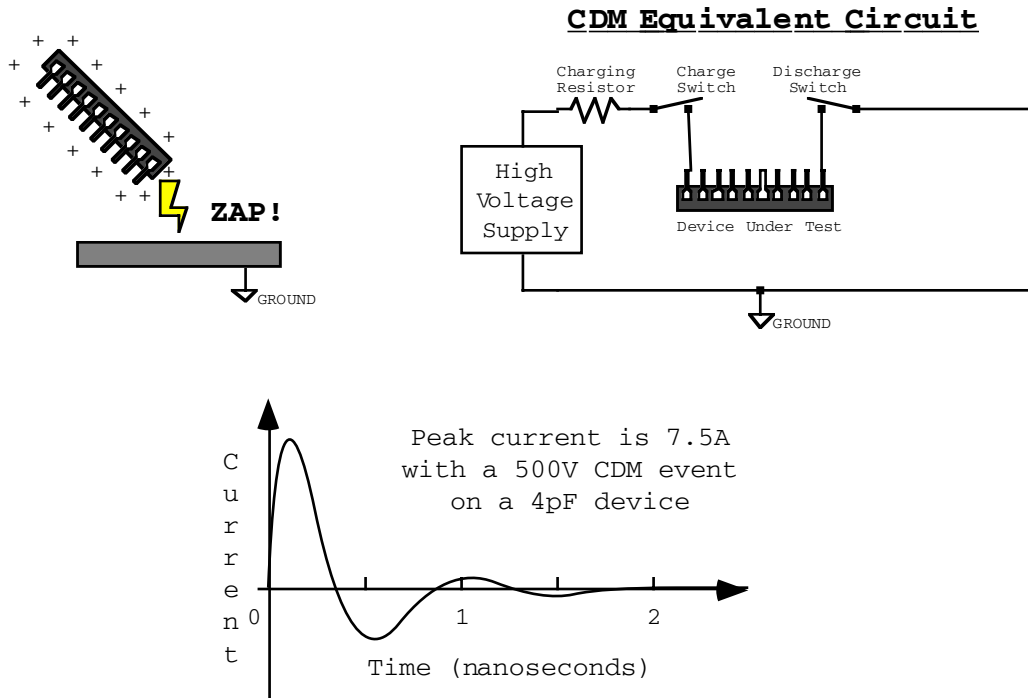
The Human Body Model (HBM) is used to approximate what happens when a person, charged up to some potential, discharges to or through an IC to ground. In this case, the human body has been modeled as a capacitor of 100pF, discharging through a series resistance of 1.5KΩ. The real world situation and the model are depicted in Figure 1. When this capacitor is charged to 2000V, it can deliver a peak current of 1.33A to the device under test! This peak occurs only ~10nsec after the event began!

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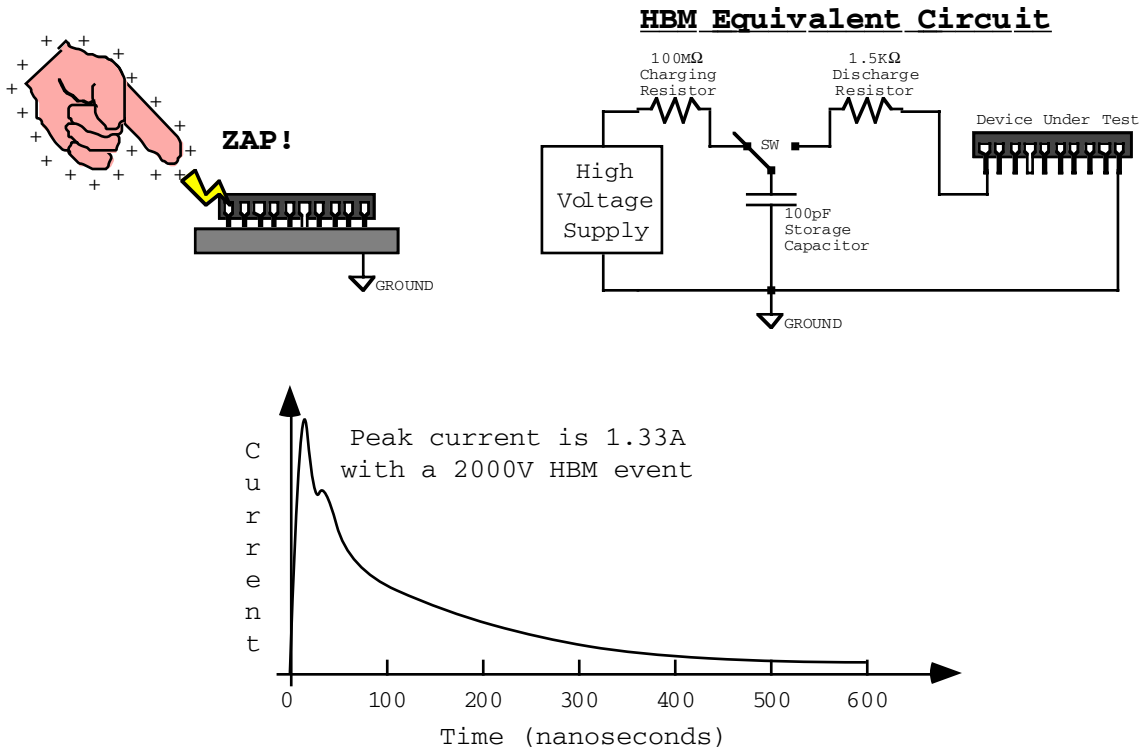
Figure 1 - *Human Body Model (HBM) stressing.*

The Machine Model (MM) is very similar to HBM, but instead of a simulated human body, a simulated machine contacts the grounded device. Since there is metal-to-metal contact, the discharge resistor is replaced by a short circuit. With no series resistance, there is more oscillation in the waveform (ringing). Total duration is about the same as with an HBM event. A 400V MM stress will impart a peak current of 7.0A to the device.

The Charged Device Model (CDM) is very different from both HBM and MM. In this case, the device itself is charged up, and discharges to ground. For instance, a device sliding out of a plastic rail will charge up via triboelectric charging if the rail isn't treated with an anti-static coating. An IC has much less capacitance than a human body, typically only a few pF, and only a small amount of charge is needed to increase the potential on a device to several hundred volts ($V=Q/C$). Any charge built up on the device discharges very quickly because of this small capacitance, as is shown in Figure 2.

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CDM Equivalent Circuit

ZAP!

GROUND

Charging Resistor   Charge Switch   Discharge Switch

High Voltage Supply

Device Under Test

GROUND

Peak current is 7.5A with a 500V CDM event on a 4pF device

Current

0   1   2

Time (nanoseconds)

Figure 2 - *Charged Device Model (CDM) stressing.*

What is Freescale's ESD Qualification Criteria?

Before any Freescale CSIC microcontroller achieves "MC" (production) status, it must demonstrate the ability to withstand repeated 2000V HBM and 200V MM stresses on all I/O pins. Each I/O pin is zapped with respect to every other pin on the chip. For example, on a 44-pin device, an I/O pin will need to be zapped 43 times, once to each of the other pins. If the device passes to the production test program following this ESD stressing, it is said to have passed ESD testing.

There is currently no specification regarding CDM susceptibility. The ESD Association, in cooperation with IEEE, is in the process of developing a standard for component level ESD sensitivity testing. The standard (#DS5.3-1993) is currently in "draft" status. Once complete, it will allow standardized testing of CDM ESD.

What are typical ESD failure modes?

Usually, a device which has failed to withstand an ESD event will have leaky or shorted pins. Because the stress enters the device through the pad, it stands to reason that the circuitry in closest proximity to this stress will fail first. Figure 3 shows a typical I/O pad configuration, and the curve traces for various types of pin failure modes. It is important to note that the

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four main failure mechanisms (discussed later) can cause any of these failure modes. Occasionally, high supply current and even functional failures can be seen on ESD failures.
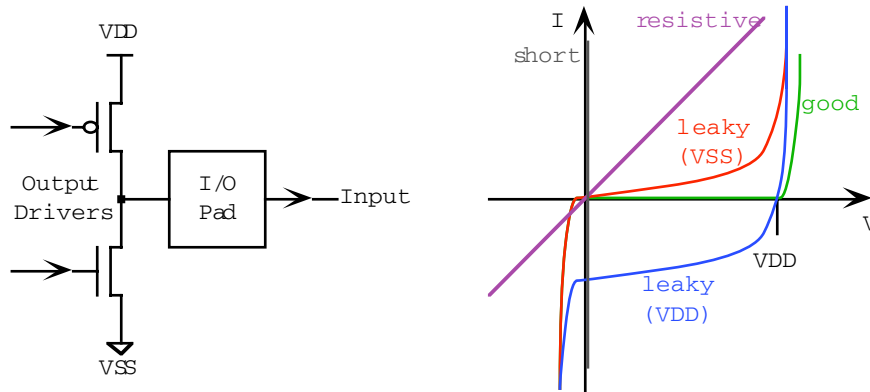
Figure 3 - *Schematic of a typical I/O pin and the curve traces of various failure modes.*

What are typical ESD failure mechanisms?

As mentioned earlier, there are four main failure mechanisms associated with ESD events. They are junction degradation, thermal oxide degradation, poly melt filaments and contact damage. All are the direct result of localized heating caused by excessive current. It is important to understand the configuration of the output buffers, and their role in the ESD event. Figure 4 shows a cross section through an I/O pad and output buffers.
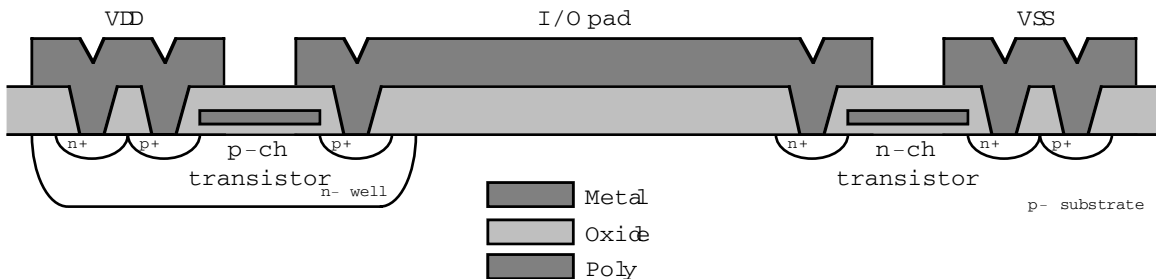
Figure 4 - *Diagram of a cross-section through an I/O pad, showing output buffers.*

The high energy pulse which is absorbed by a pin travels through the pn junctions attached to the pad, which are the drains of the output n-channel and p-channel transistors for that pin. As is typical in an ESD event, the voltage applied to the pad exceeds the reverse bias breakdown voltage of the drain junctions. Impact ionization causes high current to flow through the diode. The current (and heat generated) eventually becomes localized due to some non-uniformity in the junction processing or the device layout (i.e. the contact closest to the energy source). This increase in temperature increases the intrinsic carrier concentration, lowering the resistance along that current path. This becomes a preferential current site. More current flows here, generating more heat, lowering the intrinsic concentration, reducing the resistance, allowing more current to flow, and so on ... a positive feedback system.

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Contact damage, also called contact spiking, is the result of this particular phenomena. See Figure 5. When the excessive current causes the aluminum to heat beyond its melting point of 660C, the aluminum, which is positively charged, drifts into the substrate under the influence of the electric field. Eventually, the aluminum dopant reaches through the drain diffusion and into the substrate, shorting the drain/substrate diode, and resulting in a pad-Vss leakage path.

Junction damage can also occur in this scenario. If the heat generated by this localized current flow exceeds the melting point of silicon (1400°C), the silicon will melt and reflow, disrupting the dopant profiles in this region of the pn junction.   When the ESD event is over, the silicon recrystallizes, with the n and p-type dopants mixed up, resulting in poor isolation between p- and n- type regions, and aleaky drain/substrate diode. This type of damage is only visible after a decoration etch is performed to highlight areas of damaged silicon.   This failure mechanism is usually accompanied by other more visible mechanisms, such as contact spiking.
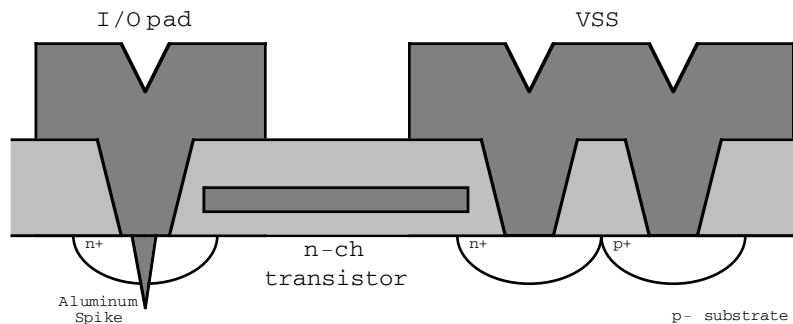
Figure 5 - Diagram of contact spiking.

Thermal oxide degradation and *poly melt filaments* are closely related failure mechanisms. Localized heating of a source/drain region can degrade the integrity of the gate oxide in the vicinity to the point of breakdown, causing a gate oxide short. If the heat generated by the high current flow from the polysilicon gate to the source/drain region reaches the melting point of silicon, then silicon from the s/d region migrates towards the gate. A "trench" is left in the junction where the silicon has been evacuated. Figure 6 is a SEM micrograph a device which has been deprocessed down to polysilicon to reveal these poly melt filaments, or "tree roots".

As mentioned earlier, more than one failure mechanism can be present on an ESD failure.   The SEM micrograph in Figure 7 shows several mechanisms which occurred as the result of a single ESD event. The unit in this case has been stripped back to silicon. A spiked contact, poly melt filament "trench" and gate oxide rupture are all present.

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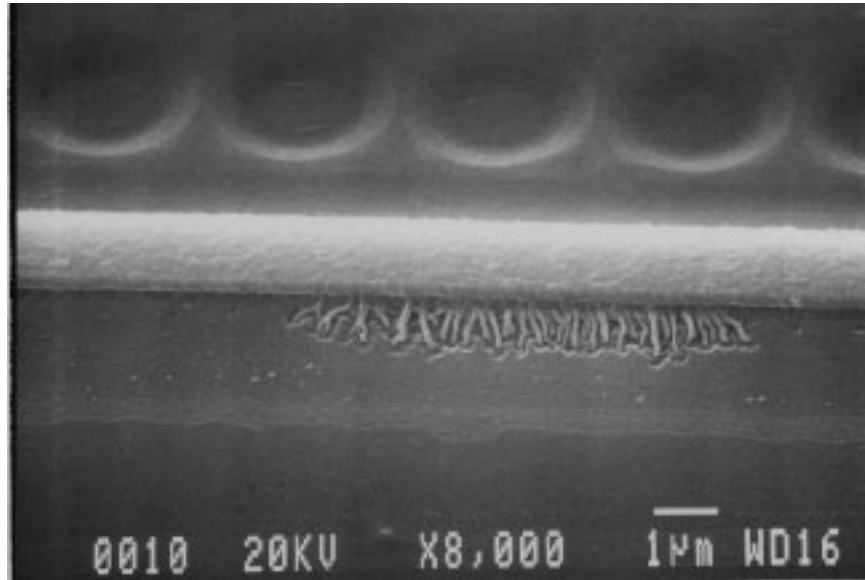
Figure 6 - *SEM micrograph of poly melt filaments. The unit has been stripped back to reveal polysilicon.*
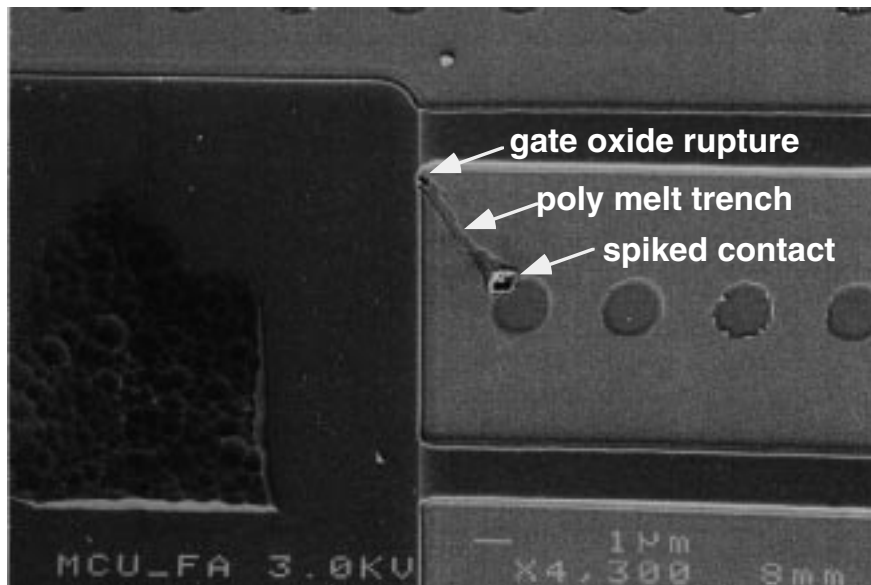
Figure 7 - *SEM micrograph showing three ESD failure mechanisms resulting from a single ESD stress. A spiked contact, poly melt trench and gate oxide short are all present.*

This technical report was compiled by Mark Thomas and Carole LeClair of Freescale's CSIC Failure Analysis Group. Please forward any questions or comments to them at the address listed above.

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