Processor
Processor.Sch

- AD[0..15]
- /SS1
- SCK1
- MOSI1
- MISO1
- /SS2
- SCK2
- MOSI2
- MISO2
- PP[0..7]
- XA[14..19]
- RS485.XMIT1
- RS485.XMIT2
- PT[0..7]
- MODC_BGND
- PM[0..7]
- SDA.I2C
- SCL.I2C
- RTC.CS_CLEANUP
- SCK0_/MASTER2
- MOSI0_/SUPPRESS.BOOT.V
- MISO0
- PS3.TXD1
- PS2.RXD1
- PS1.TXD0
- PS0.RXD0
- AN[0..15]
- /XIRQ
- /IRQ
- R//W
- /LSTRB
- E
- MODA
- MODB
- 16MHZ
- I.AD[0..15]
- /HC12.RESET

Logic
Logic.Sch

- RAM.WRITE
- E
- R//W
- /XFLASH.CS
- TDI
- TMS
- TCK
- A[0..13]
- XA[14..19]
- TDO
- RAM.CS
- /RAM.OE
- /MOD.WE
- /MOD.OE
- 16MHZ
- MOD.R//W
- MOD.E
- /MOD0.CS
- /MOD1.CS
- F.LOW.ADDR.LATCH
- F.HIGH.ADDR.LATCH
- /RAM1.CS
- EDELAY.LATCH
- E
- I.AD[0..15]
- MOD.AD[0..7]

RAM
RAM.sch

- I.AD[0..15]
- R//W
- XA[14..19]
- /RAM.OE
- /LSTRB
- /RAM1.CS
- E
- RAM.WRITE
- AD[0..15]
- RAM.CS
- EDELAY.LATCH
- A[0..13]
- D[0..15]
- E

XFlash
XFlash.Sch

- A[0..13]
- MOD.AD[0..7]
- F.LOW.ADDR.LATCH
- F.HIGH.ADDR.LATCH
- FLASH.A[0..18]
- /MOD.WE
- /MOD.OE
- /XFLASH.CS

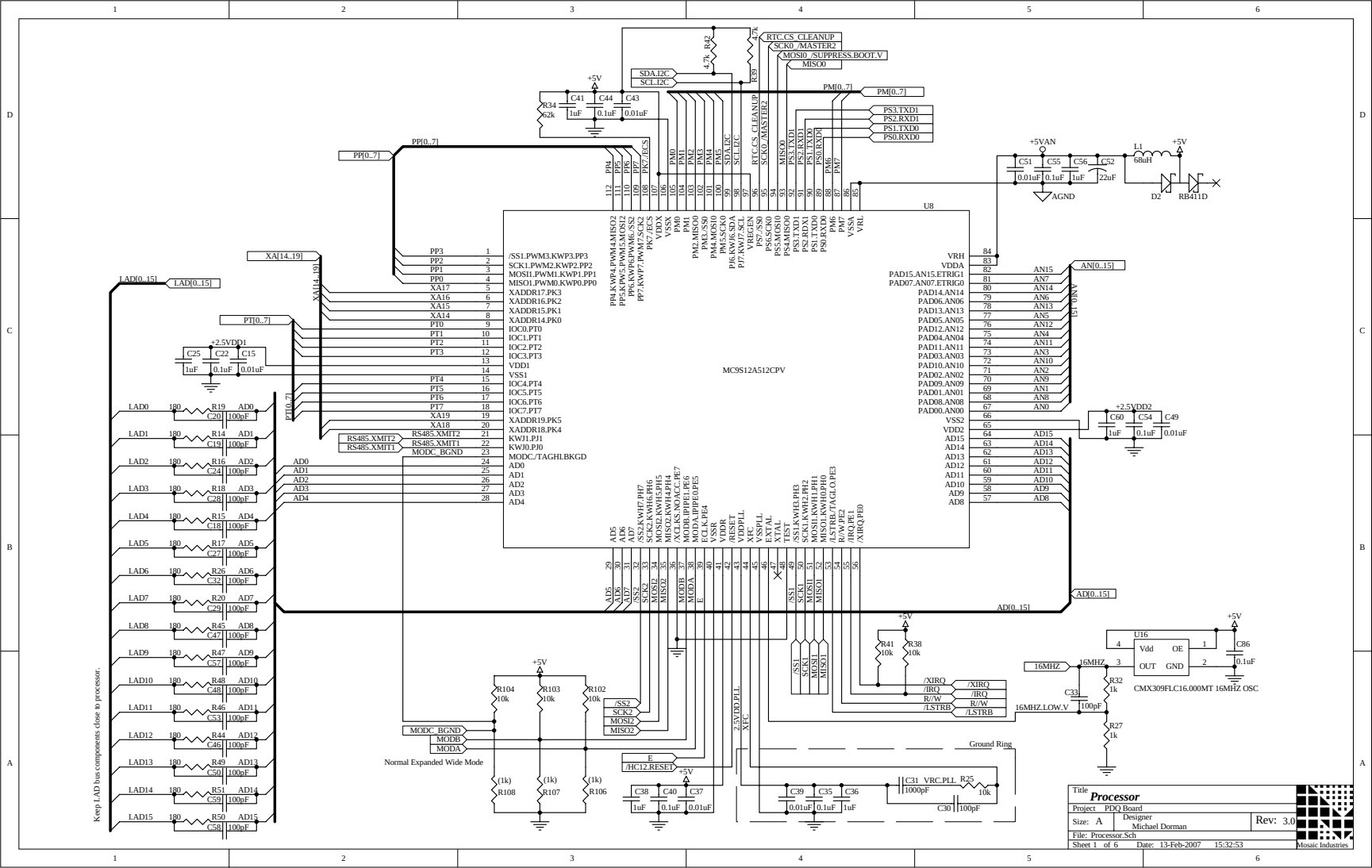
Serial_Reset_RTC
Serial_Reset_RTC.Sch

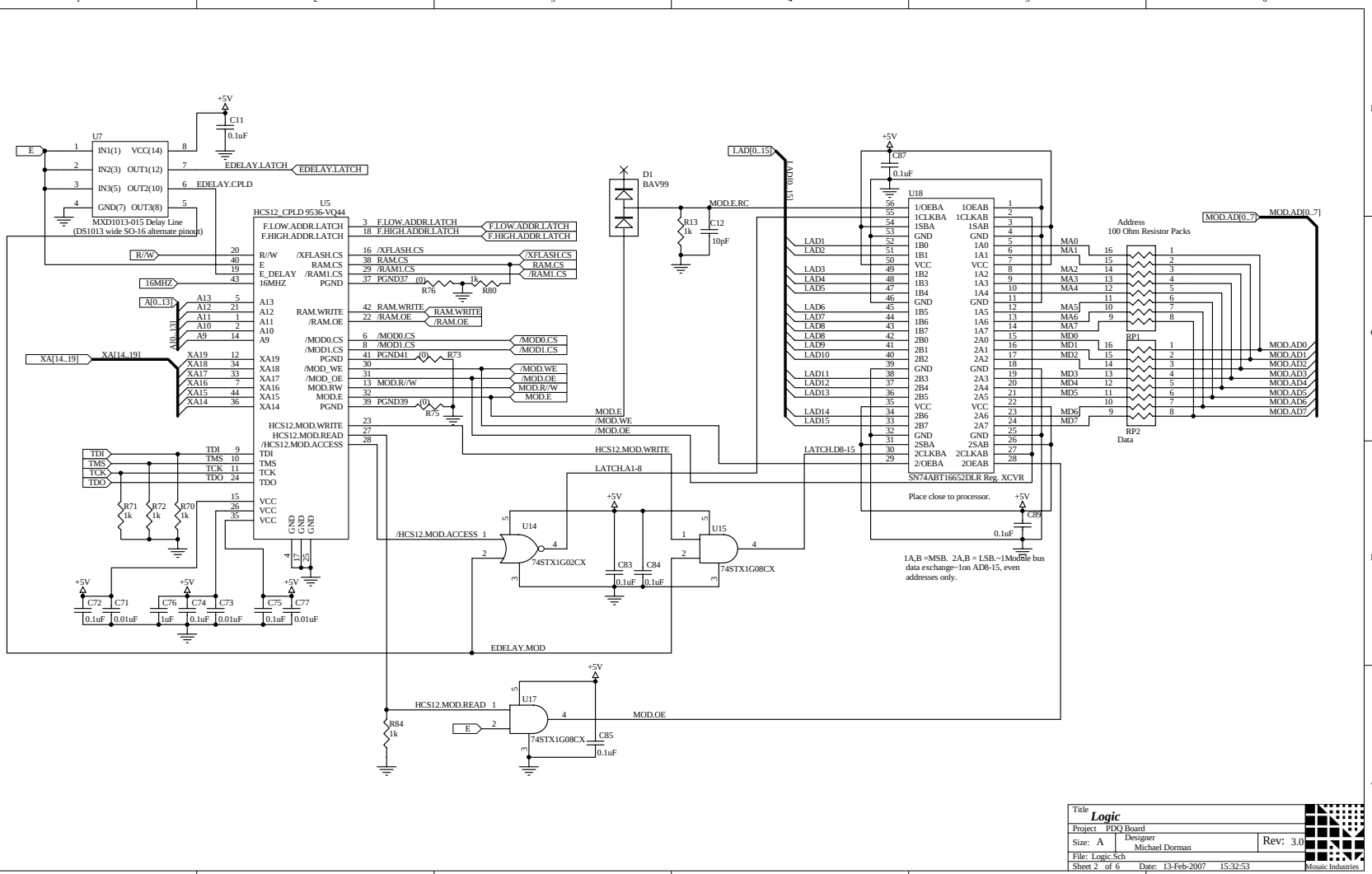
- /TXD1
- /RXD2
- XCV1+
- XCV1-
- /RXD1
- /TXD2
- /HC12.RESET
- /RESET
- VBAT
- MISO0
- SCK0_/MASTER2
- AN[0..15]
- PS3.TXD1
- PS2.RXD1
- PS1.TXD0
- PS0.RXD0
- RS485.XMIT1
- RS485.XMIT2
- XCV2+
- XCV2-
- RTC.CS_CLEANUP
- MOSI0_/SUPPRESS.BOOT.V

Headers
Headers.Sch

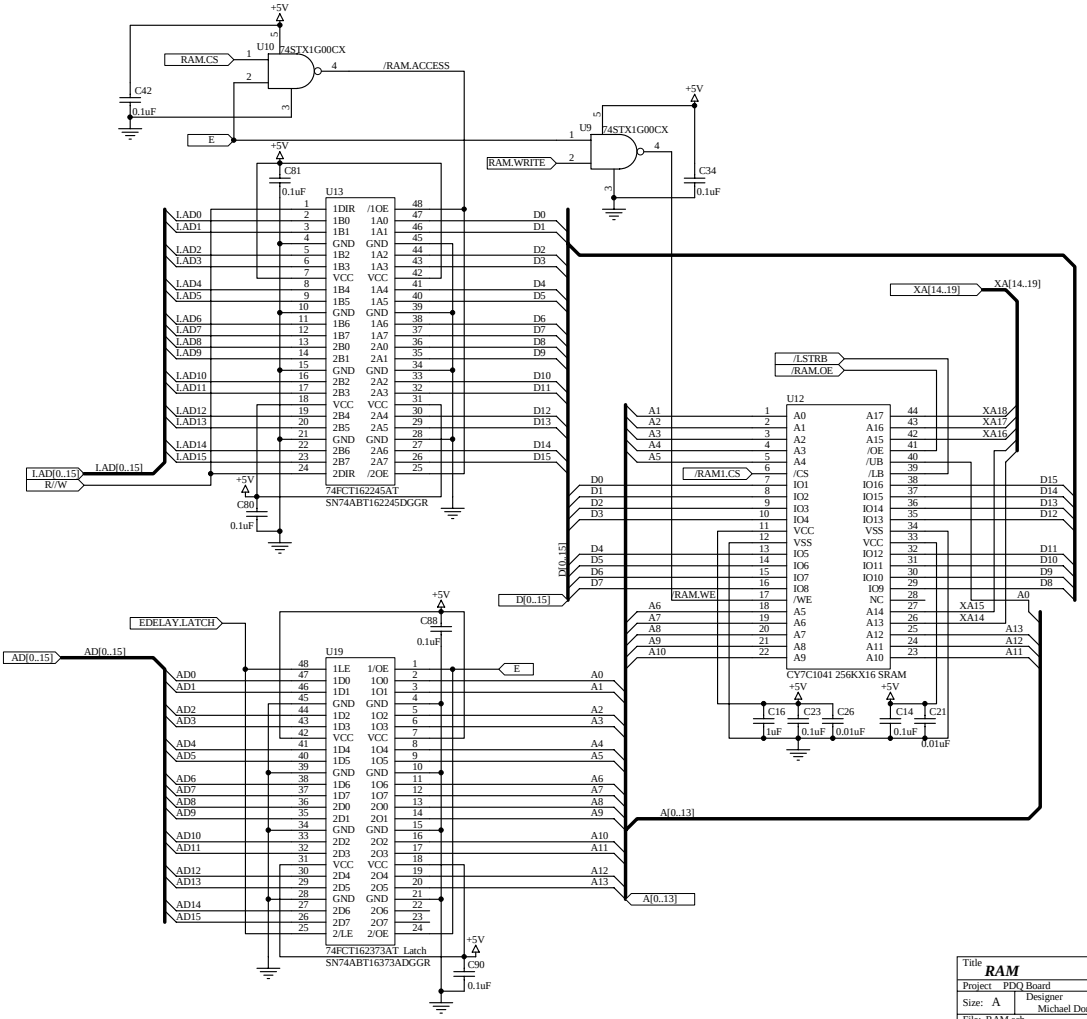
- MOD_AD[0..7]
- AN[0..15]
- /MOD1.CS
- MISO0
- /RESET
- /MOD.WE
- /MOD.OE
- MOD.R//W
- MOD.E
- /IRQ
- FLASH.A8
- FLASH.A9
- 16MHZ
- V+RAW
- PP[0..7]
- PT[0..7]
- SDA.I2C
- SCL.I2C
- V+RAW
- PM[0..7]
- TMS
- TCK
- TDO
- TDI
- V+RAW
- /TXD1
- /TXD2
- XCV1-
- /RXD1
- XCV1+
- /RXD2
- XCV2-
- XCV2+
- /XIRQ
- /SS1
- SCK1
- MOSI1
- MISO1
- /SS2
- SCK2
- MOSI2
- MISO2
- MODC_BGND
- MODB
- E
- MODA
- /RESET
- MISO0
- /MOD.WE
- MOD.R//W
- FLASH.A8
- 16MHZ
- /MOD0.CS
- /RESET
- /MOD.OE
- MOD.E
- /IRQ
- FLASH.A9
- /MOD1.CS
- VBAT
- SCK0_/MASTER2
- MOSI0_/SUPPRESS.BOOT.V
- SCK0_/MASTER2
- MOSI0_/SUPPRESS.BOOT.V

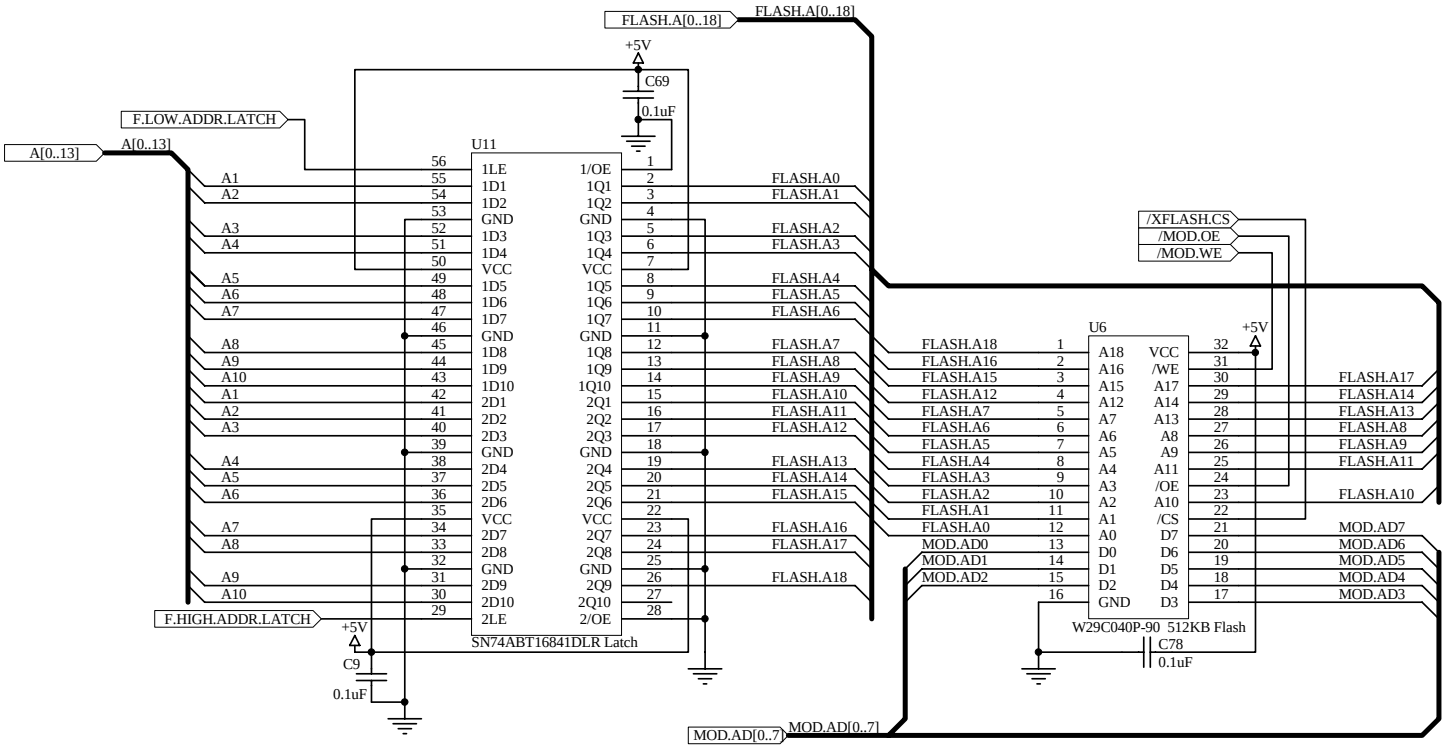
Title	***Schematic Overview***	
Project	PDQ Board	
Size: A	Designer: Michael Dorman	Rev: 3.0
File: HCS12.prj		
Sheet 1 of 1	Date: 13-Feb-2007 15:32:52	Mosaic Industries


RTC.CS_CLEANUP
SCK0_/MASTER2
MOSI0_/SUPPRESS.BOOT.V
MISO0
4.7k_R42
4.7k
R89
SDA.I2C
SCL.I2C
+5V
R34 62k
C41 1uF
C44 0.1uF
C43 0.01uF
PM[0..7]
PS3.TXD1
PS2.RXD1
PS1.TXD0
PS0.RXD0
PP[0..7]
PM0
PM1
PM2
PM3
PM4
PM5
SDA.I2C
SCL.I2C
PM6
PM7
+5VAN
C51 0.01uF
C55 0.1uF
C56 1uF
C52 22uF
L1 68uH
+5V
AGND
D2 RB411D
U8
MC9S12A512CPV
PP3
PP2
PP1
PP0
XA17
XA16
XA15
XA14
PT0
PT1
PT2
PT3
PT4
PT5
PT6
PT7
XA19
XA18
RS485.XMIT2
RS485.XMIT1
MODC_BGND
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
/SS2
SCK2
MOSI2
MISO2
MODB
MODA
E
/HC12.RESET
VRH
VDDA
PAD15.AN15.ETRIG1
PAD07.AN07.ETRIG0
PAD14.AN14
PAD06.AN06
PAD13.AN13
PAD05.AN05
PAD12.AN12
PAD04.AN04
PAD11.AN11
PAD03.AN03
PAD10.AN10
PAD02.AN02
PAD09.AN09
PAD01.AN01
PAD08.AN08
PAD00.AN00
VSS2
VDD2
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AN[0..15]
5V ONLY
+2.5VDD2
C60 1uF
C54 0.1uF
C49 0.01uF
+2.5VDD1
C25 1uF
C22 0.1uF
C15 0.01uF
XA[14..19]
LAD[0..15]
PT[0..7]
AD[0..15]
LAD0 180 R19 C20 100pF AD0
LAD1 180 R14 C19 100pF AD1
LAD2 180 R16 C24 100pF AD2
LAD3 180 R18 C28 100pF AD3
LAD4 180 R15 C18 100pF AD4
LAD5 180 R17 C27 100pF AD5
LAD6 180 R26 C32 100pF AD6
LAD7 180 R20 C29 100pF AD7
LAD8 180 R45 C47 100pF AD8
LAD9 180 R47 C57 100pF AD9
LAD10 180 R48 C48 100pF AD10
LAD11 180 R46 C53 100pF AD11
LAD12 180 R44 C46 100pF AD12
LAD13 180 R49 C50 100pF AD13
LAD14 180 R51 C59 100pF AD14
LAD15 180 R50 C58 100pF AD15
Keep LAD bus components close to processor.
R104 10k
R103 10k
R102 10k
/SS2
SCK2
MOSI2
MISO2
MODC_BGND
MODB
MODA
Normal Expanded Wide Mode
(1k) R108
(1k) R107
(1k) R106
R41 10k
R38 10k
/SS1
SCK1
MOSI1
MISO1
/XIRQ
/IRQ
R/W
/LSTRB
16MHZ.LOW.V
U16
Vdd
OUT
OE
GND
C86 0.1uF
16MHZ
R32 1k
C33 100pF
R27 1k
CMX309FLC16.000MT 16MHZ OSC
Ground Ring
C38 1uF
C40 0.1uF
C37 0.01uF
C39 0.01uF
C35 0.1uF
C36 1uF
C31 VRC.PLL 1000pF
R25 10k
C30 100pF
2.5VDD.PLL
XFC
Title Processor
Project PDQ Board
Size: A
Designer Michael Dorman
Rev: 3.0
File: Processor.Sch
Sheet 1 of 6
Date: 13-Feb-2007 15:32:53
Mosaic Industries

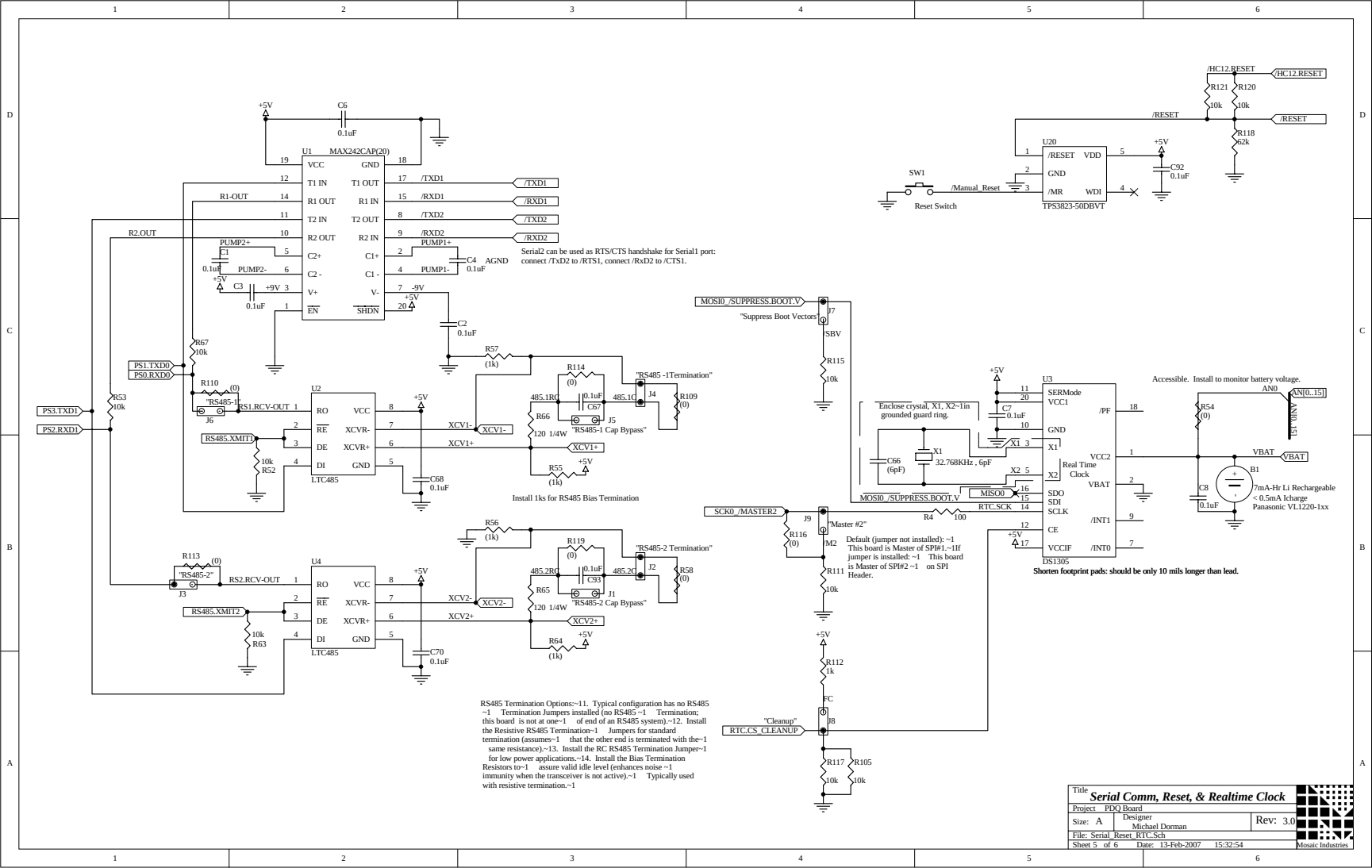


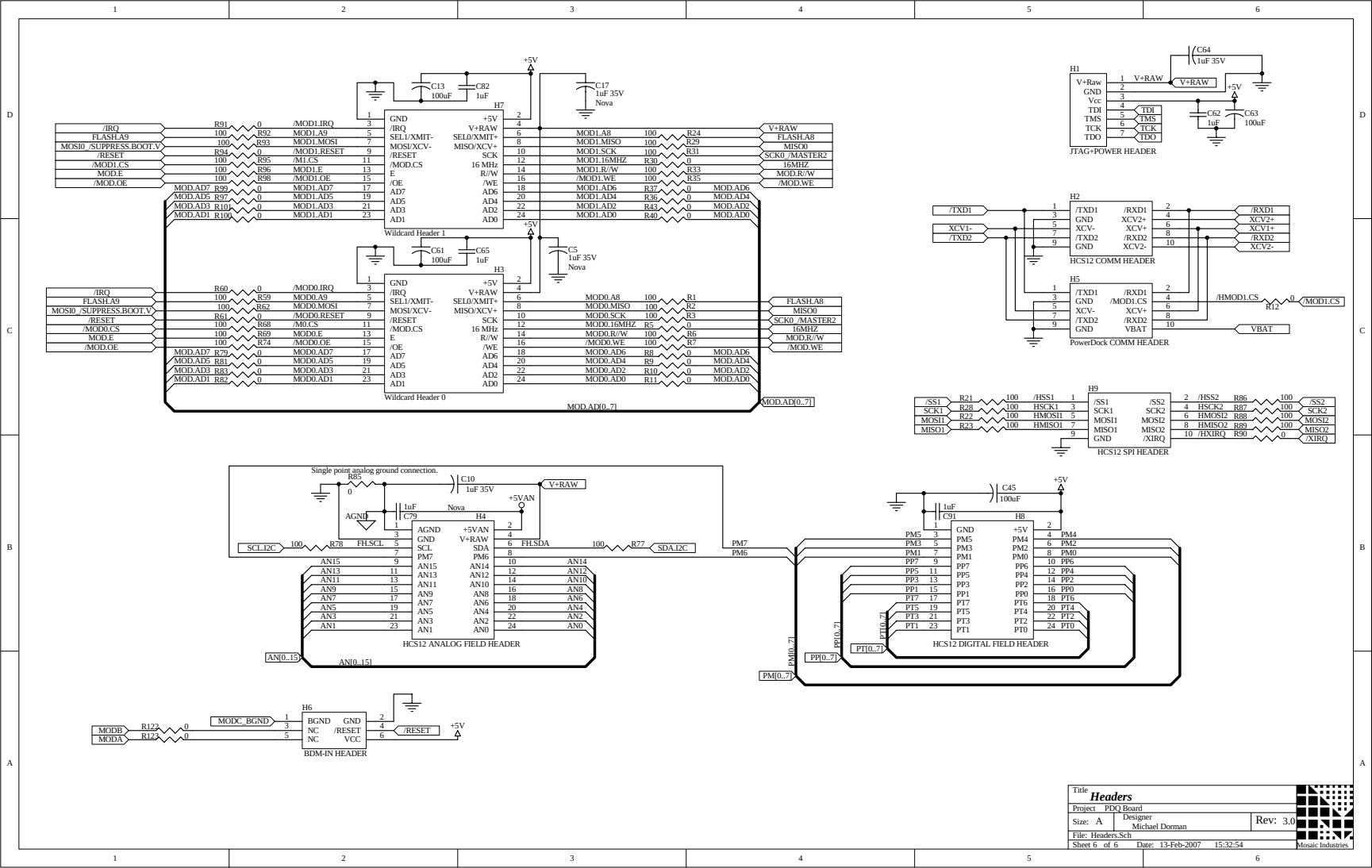
Title	**Logic**
Project	PDQ Board
Size: A	Designer: Michael Dorman
Rev: 3.0	
File: Logic.Sch	
Sheet 2 of 6	Date: 13-Feb-2007 15:32:53
Mosaic Industries	


+5V
U10
74STX1G00CX
RAM.CS
/RAM.ACCESS
C42
0.1uF
E
U9
74STX1G00CX
RAM.WRITE
C34
0.1uF
C81
0.1uF
U13
LAD0
LAD1
LAD2
LAD3
LAD4
LAD5
LAD6
LAD7
LAD8
LAD9
LAD10
LAD11
LAD12
LAD13
LAD14
LAD15
LAD[0..15]
R/W
C80
0.1uF
74FCT162245AT
SN74ABT162245DGGR
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D[0..15]
XA[14..19]
/LSTRB
/RAM.OE
U12
/RAM1.CS
/RAM.WE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
XA14
XA15
XA16
XA17
XA18
CY7C1041 256KX16 SRAM
C16
1uF
C23
0.1uF
C26
0.01uF
C14
0.1uF
C21
0.01uF
EDELAY.LATCH
AD[0..15]
C88
0.1uF
U19
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
74FCT162373AT Latch
SN74ABT16373ADGGR
A[0..13]
C90
0.1uF
Title
RAM
Project PDQ Board
Size: A
Designer
Michael Dorman
Rev: 3.0
File: RAM.sch
Sheet 3 of 6
Date: 13-Feb-2007 15:32:53
Mosaic Industries



Title	***External Flash***	
Project	PDQ Board	
Size: A	Designer: Michael Dorman	Rev: 3.0
File: XFlash.Sch		
Sheet 4 of 6	Date: 13-Feb-2007 15:32:53	Mosaic Industries


U1 MAX242CAP(20)
VCC GND
T1 IN T1 OUT
R1 OUT R1 IN
T2 IN T2 OUT
R2 OUT R2 IN
C2+ C1+
C2 - C1 -
V+ V-
EN SHDN
/TXD1
/RXD1
/TXD2
/RXD2
PUMP1+
PUMP1-
PUMP2+
PUMP2-
+5V
+9V
-9V
C1 0.1uF
C2 0.1uF
C3 0.1uF
C4 0.1uF
C6 0.1uF
AGND
R1-OUT
R2.OUT
Serial2 can be used as RTS/CTS handshake for Serial1 port:
connect /TxD2 to /RTS1, connect /RxD2 to /CTS1.
R67 10k
PS1.TXD0
PS0.RXD0
R110 (0)
"RS485-1"
J6
RS1.RCV-OUT
PS3.TXD1
PS2.RXD1
R53 10k
RS485.XMIT1
10k R52
U2
RO VCC
RE XCVR-
DE XCVR+
DI GND
LTC485
C68 0.1uF
XCV1-
XCV1+
R57 (1k)
R114 (0)
"RS485 -1Termination"
485.1RC
485.1C
C67 0.1uF
J4
J5
R109 (0)
R66 120 1/4W
"RS485-1 Cap Bypass"
R55 (1k)
Install 1ks for RS485 Bias Termination
R113 (0)
"RS485-2"
J3
RS2.RCV-OUT
RS485.XMIT2
10k R63
U4
C70 0.1uF
XCV2-
XCV2+
R56 (1k)
R119 (0)
"RS485-2 Termination"
485.2RC
485.2C
C93 0.1uF
J2
J1
R58 (0)
R65 120 1/4W
"RS485-2 Cap Bypass"
R64 (1k)
RS485 Termination Options:~11. Typical configuration has no RS485
~1 Termination Jumpers installed (no RS485 ~1 Termination;
this board is not at one~1 of end of an RS485 system).~12. Install
the Resistive RS485 Termination~1 Jumpers for standard
termination (assumes~1 that the other end is terminated with the~1
same resistance).~13. Install the RC RS485 Termination Jumper~1
for low power applications.~14. Install the Bias Termination
Resistors to~1 assure valid idle level (enhances noise ~1
immunity when the transceiver is not active).~1 Typically used
with resistive termination.~1
/HC12.RESET
/HC12.RESET
R121 10k
R120 10k
/RESET
/RESET
R118 62k
U20
/RESET VDD
GND
/MR WDI
TPS3823-50DBVT
C92 0.1uF
SW1
/Manual_Reset
Reset Switch
MOSI0_/SUPPRESS.BOOT.V
"Suppress Boot Vectors"
J7
SBV
R115 10k
Enclose crystal, X1, X2~1in
grounded guard ring.
C66 (6pF)
X1
32.768KHz , 6pF
U3
SERMode
VCC1
GND
X1
X2
Real Time
Clock
SDO
SDI
SCLK
CE
VCCIF
/PF
/INT1
/INT0
VBAT
DS1305
C7 0.1uF
MISO0
MOSI0_/SUPPRESS.BOOT.V
RTC.SCK
R4 100
Accessible. Install to monitor battery voltage.
AN0
AN[0..15]
R54 (0)
VBAT
B1
C8 0.1uF
7mA-Hr Li Rechargeable
< 0.5mA Icharge
Panasonic VL1220-1xx
Shorten footprint pads: should be only 10 mils longer than lead.
SCK0_/MASTER2
J9
M2
Master #2"
Default (jumper not installed): ~1
This board is Master of SPI#1.~1If
jumper is installed: ~1 This board
is Master of SPI#2 ~1 on SPI
Header.
R116 (0)
R111 10k
R112 1k
FC
J8
"Cleanup"
RTC.CS_CLEANUP
R117 10k
R105 10k
Title
Serial Comm, Reset, & Realtime Clock
Project PDQ Board
Size: A
Designer
Michael Dorman
Rev: 3.0
File: Serial_Reset_RTC.Sch
Sheet 5 of 6
Date: 13-Feb-2007 15:32:54
Mosaic Industries


H7
Wildcard Header 1
H3
Wildcard Header 0
MOD.AD[0..7]
H1
JTAG+POWER HEADER
H2
HCS12 COMM HEADER
H5
PowerDock COMM HEADER
H9
HCS12 SPI HEADER
Single point analog ground connection.
HCS12 ANALOG FIELD HEADER
HCS12 DIGITAL FIELD HEADER
H6
BDM-IN HEADER
Title Headers
Project PDQ Board
Size: A
Designer Michael Dorman
Rev: 3.0
File: Headers.Sch
Sheet 6 of 6
Date: 13-Feb-2007 15:32:54
Mosaic Industries