30A, 60V, ESD Rated, 0.047 Ohm, Logic Level N-Channel Power MOSFETs

These are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

These transistors incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

Formerly developmental type TA49027.

Features

- 30A, 60V
- $r_{DS(ON)} = 0.047\, \Omega$
- 2kV ESD Protected
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

Ordering Information

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<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BRAND</th>
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<tr>
<td>RFP30N06LE</td>
<td>TO-220AB</td>
<td>F30N06LE</td>
</tr>
<tr>
<td>RF1S30N06LESM</td>
<td>TO-263AB</td>
<td>1S30N06L</td>
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</table>

NOTE: When ordering use the entire part number. Add suffix, 9A, to obtain the TO-263 variant in tape and reel i.e. RF1S30N06LESM9A.
**Absolute Maximum Ratings**  \( T_A = 25^\circ C, \) Unless Otherwise Specified

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>MAX</th>
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<tbody>
<tr>
<td>Drain to Source Voltage (Note 1)</td>
<td>( V_{DSS} )</td>
<td>( I_D = 250\mu A, \ V_{GS} = 0V, ) Figure 11</td>
<td>60</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Gate to Threshold Voltage</td>
<td>( V_{GS(TH)} )</td>
<td>( V_{DS} = 2V, \ I_D = 250\mu A, ) Figure 10</td>
<td>1</td>
<td>-</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>( I_{DS} )</td>
<td>( V_{DS} = ) Rated ( V_{DSS} ), ( V_{GS} = 0 )</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td>( V_{DS} = 0.8 \times ) Rated ( V_{DSS} ), ( V_{GS} = 0 ), ( T_C = 150^\circ C )</td>
<td>-</td>
<td>-</td>
<td>250</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>Gate to Source Leakage Current</td>
<td>( I_{GSS} )</td>
<td>( V_{GS} = +10, -8V )</td>
<td>-</td>
<td>-</td>
<td>±10</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Drain to Source On Resistance (Note 2)</td>
<td>( I_{DS(ON)} )</td>
<td>( I_D = 30A, \ V_{GS} = 5V, ) Figure 9</td>
<td>-</td>
<td>-</td>
<td>0.047</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Turn-On Time</td>
<td>( I_{ON} )</td>
<td>( V_{DD} = 30V, \ I_D = 30A, ) ( R_L = 1\Omega, \ V_{GS} = 5V, ) ( R_G = 2.5\Omega, ) ( V_{DS} = 2.5V, ) Figures 13, 16, 17</td>
<td>-</td>
<td>-</td>
<td>140</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>( I_{d(ON)} )</td>
<td></td>
<td>-</td>
<td>11</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>( t_r )</td>
<td></td>
<td>-</td>
<td>88</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>( I_{d(OFF)} )</td>
<td></td>
<td>-</td>
<td>30</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Fall Time</td>
<td>( I_f )</td>
<td></td>
<td>-</td>
<td>40</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-Off Time</td>
<td>( I_{OFF} )</td>
<td></td>
<td>-</td>
<td>100</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Total Gate Charge</td>
<td>( Q_{g(TOT)} )</td>
<td>( V_{GS} = 0V ) to 10V</td>
<td>-</td>
<td>51</td>
<td>62</td>
<td>nC</td>
</tr>
<tr>
<td>Gate Charge at 5V</td>
<td>( Q_{g(5)} )</td>
<td>( V_{GS} = 0V ) to 5V</td>
<td>-</td>
<td>28</td>
<td>34</td>
<td>nC</td>
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<tr>
<td>Threshold Gate Charge</td>
<td>( Q_{g(TH)} )</td>
<td>( V_{GS} = 0V ) to 1V</td>
<td>-</td>
<td>1.8</td>
<td>2.6</td>
<td>nC</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>( V_{DS} = 25V, \ V_{GS} = 0V, ) ( f = 1MHz, ) Figures 18, 19</td>
<td>-</td>
<td>1350</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>( C_{OSS} )</td>
<td>( V_{DS} = 25V, \ V_{GS} = 0V, ) ( f = 1MHz, ) Figure 12</td>
<td>-</td>
<td>290</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>( C_{RSS} )</td>
<td></td>
<td>-</td>
<td>85</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Thermal Resistance Junction to Case</td>
<td>( R_{RJC} )</td>
<td></td>
<td>-</td>
<td>-</td>
<td>1.55</td>
<td>°C/W</td>
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<tr>
<td>Thermal Resistance Junction to Ambient</td>
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<td></td>
<td>-</td>
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<td>°C/W</td>
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**Source to Drain Diode Specifications**

<table>
<thead>
<tr>
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<tr>
<td>Source to Drain Diode Voltage (Note 2)</td>
<td>( V_{SD} )</td>
<td>( I_{SD} = 30A )</td>
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<td>1.5</td>
<td>V</td>
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<tr>
<td>Diode Reverse Recovery Time</td>
<td>( t_r )</td>
<td>( I_{SD} = 30A, ) ( dI_{SD}/dt = 100A/\mu s )</td>
<td>-</td>
<td>-</td>
<td>125</td>
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</table>

**ELECTROSTATIC DISCHARGE RATING,MIL-STD-883,CATEGORY B(2) ESD 2 kV**

**CAUTION:** Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**
1. \( T_J = 25^\circ C \) to 150°C.

**Electrical Specifications**  \( T_C = 25^\circ C, \) Unless Otherwise Specified

<table>
<thead>
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<td>-</td>
<td>-</td>
<td>80</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

**NOTES:**
2. Pulse Test: Pulse Width ≤ 300ms, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse Width limited by max junction temperature. See Transient Thermal Impedance Curve (Figure 3) and Peak Current Capability Curve (Figure 5).
Typical Performance Curves  Unless Otherwise Specified

**FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE**

**FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE**

**FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE**

**FIGURE 4. FORWARD BIAS SAFE OPERATING AREA**

**FIGURE 5. PEAK CURRENT CAPABILITY**
Typical Performance Curves Unless Otherwise Specified (Continued)

![Figure 6. Unclamped Inductive Switching](image)

![Figure 7. Saturation Characteristics](image)

![Figure 8. Transfer Characteristics](image)

![Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature](image)

![Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature](image)

![Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature](image)

NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

\[ t_{AV} = \begin{cases} \frac{(L)(I_{AS})(1.3^{*RATED \ BV_{DSS}} - V_{DD})}{I_{AS}} & \text{if } R = 0 \\ \frac{(L/R) \ln\left(\frac{(I_{AS}R)(1.3^{*RATED \ BV_{DSS}} - V_{DD})}{1+1}\right)}{I_{AS}} & \text{if } R \neq 0 \end{cases} \]

STARTING \( T_J = 25^\circ C \)

STARTING \( T_J = 150^\circ C \)

\( I_{AV} \), AVALANCHE CURRENT (A)

\( I_{AS} \), AVALANCHE CURRENT (A)

\( I_{DS(ON)} \), DRAIN TO SOURCE CURRENT (A)

\( V_{GS} \), GATE TO SOURCE VOLTAGE (V)

\( V_{DS} \), DRAIN TO SOURCE VOLTAGE (V)

\( V_{DD} = 15V \)

\( V_{GS} = 3V \)

\( V_{GS} = 4V \)

\( V_{GS} = 5V \)

\( V_{GS} = 6V \)

\( V_{GS} = 7V \)

\( V_{GS} = 8V \)

\( V_{GS} = 9V \)

\( V_{GS} = 10V \)

\( V_{DS} = \text{DRAIN TO SOURCE VOLTAGE (V)} \)

\( V_{DD} = \text{DRAIN TO SOURCE VOLTAGE (V)} \)

\( V_{GS} = \text{GATE TO SOURCE VOLTAGE (V)} \)

\( V_{DS} = \text{DRAIN TO SOURCE VOLTAGE (V)} \)

\( T_J, \text{JUNCTION TEMPERATURE (°C)} \)

\( PULSE \ DURATION = 80\mu s \)

DUTY CYCLE = 0.5% MAX.

\( DUTY \ CYCLE = 0.5\% \ MAX. \)

\( V_{DD} = 15V \)

\( PULSE \ DURATION = 80\mu s \)

\( V_{GS} = 5V \)

\( V_{GS} = 4.5V \)

\( V_{GS} = 4V \)

\( V_{GS} = 3V \)

\( V_{GS} = 2V \)

\( V_{GS} = 1V \)

\( V_{GS} = 0V \)

\( V_{GS} = -1V \)

\( V_{GS} = -2V \)

\( V_{GS} = -3V \)

\( V_{GS} = -4V \)

\( V_{GS} = -5V \)

\( V_{GS} = -6V \)

\( V_{GS} = -7V \)

\( V_{GS} = -8V \)

\( V_{GS} = -9V \)

\( V_{GS} = -10V \)

\( V_{GS} = -11V \)

\( V_{GS} = -12V \)

\( V_{GS} = -13V \)

\( V_{GS} = -14V \)

\( V_{GS} = -15V \)

\( V_{GS} = -16V \)

\( V_{GS} = -17V \)

\( V_{GS} = -18V \)

\( V_{GS} = -19V \)

\( V_{GS} = -20V \)

\( V_{GS} = -21V \)

\( V_{GS} = -22V \)

\( V_{GS} = -23V \)

\( V_{GS} = -24V \)

\( V_{GS} = -25V \)

\( V_{GS} = -26V \)

\( V_{GS} = -27V \)

\( V_{GS} = -28V \)

\( V_{GS} = -29V \)

\( V_{GS} = -30V \)

\( V_{GS} = -31V \)

\( V_{GS} = -32V \)

\( V_{GS} = -33V \)

\( V_{GS} = -34V \)

\( V_{GS} = -35V \)

\( V_{GS} = -36V \)

\( V_{GS} = -37V \)

\( V_{GS} = -38V \)

\( V_{GS} = -39V \)

\( V_{GS} = -40V \)

\( V_{GS} = -41V \)

\( V_{GS} = -42V \)

\( V_{GS} = -43V \)

\( V_{GS} = -44V \)

\( V_{GS} = -45V \)

\( V_{GS} = -46V \)

\( V_{GS} = -47V \)

\( V_{GS} = -48V \)

\( V_{GS} = -49V \)

\( V_{GS} = -50V \)

\( V_{GS} = -51V \)

\( V_{GS} = -52V \)

\( V_{GS} = -53V \)

\( V_{GS} = -54V \)

\( V_{GS} = -55V \)

\( V_{GS} = -56V \)

\( V_{GS} = -57V \)

\( V_{GS} = -58V \)

\( V_{GS} = -59V \)

\( V_{GS} = -60V \)

\( V_{GS} = -61V \)

\( V_{GS} = -62V \)

\( V_{GS} = -63V \)

\( V_{GS} = -64V \)

\( V_{GS} = -65V \)

\( V_{GS} = -66V \)

\( V_{GS} = -67V \)

\( V_{GS} = -68V \)

\( V_{GS} = -69V \)

\( V_{GS} = -70V \)

\( V_{GS} = -71V \)

\( V_{GS} = -72V \)

\( V_{GS} = -73V \)

\( V_{GS} = -74V \)

\( V_{GS} = -75V \)

\( V_{GS} = -76V \)

\( V_{GS} = -77V \)

\( V_{GS} = -78V \)

\( V_{GS} = -79V \)

\( V_{GS} = -80V \)

\( V_{GS} = -81V \)

\( V_{GS} = -82V \)

\( V_{GS} = -83V \)

\( V_{GS} = -84V \)

\( V_{GS} = -85V \)

\( V_{GS} = -86V \)

\( V_{GS} = -87V \)

\( V_{GS} = -88V \)

\( V_{GS} = -89V \)

\( V_{GS} = -90V \)

\( V_{GS} = -91V \)

\( V_{GS} = -92V \)

\( V_{GS} = -93V \)

\( V_{GS} = -94V \)

\( V_{GS} = -95V \)

\( V_{GS} = -96V \)

\( V_{GS} = -97V \)

\( V_{GS} = -98V \)

\( V_{GS} = -99V \)

\( V_{GS} = -100V \)
**Typical Performance Curves**  Unless Otherwise Specified  (Continued)

**FIGURE 12.** CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

**FIGURE 13.** NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

**Test Circuits and Waveforms**

**FIGURE 14.** UNCLAMPED ENERGY TEST CIRCUIT

**FIGURE 15.** UNCLAMPED ENERGY WAVEFORMS

**FIGURE 16.** SWITCHING TIME TEST CIRCUIT

**FIGURE 17.** RESISTIVE SWITCHING WAVEFORMS

NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.
Test Circuits and Waveforms (Continued)

**FIGURE 18. GATE CHARGE TEST CIRCUIT**

**FIGURE 19. GATE CHARGE WAVEFORMS**
PSPICE Electrical Model

SUBCKT RFP30N06LE 2 1 3; rev 6/2/93
CA 1 2 8 1 3.34e-9
CB 1 5 14 3.44e-9
CIN 6 8 0 1.34e-9

DBODY 7 5 DBDMOD
DBREAK 11 5 DBKMOD
DESD1 9 1 5 DESD1MOD
DESD2 9 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 75.39
EDS 14 5 8 1
EGS 6 10 8 1
EVTO 20 6 18 8 1

IT 8 17 1
LDRAIN 2 5 1e-9
LGATE 1 9 7.22e-9
LSOURCE 3 7 6.31e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 11.86e-3
RGATE 9 20 2.52
RIN 6 8 1e9
RSCL1 5 51 RSLVCMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 26.6e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 8 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.5

ESCL 51 50 VALUE = ((V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/89,7))

.MODEL DBDMOD D (IS = 3.80e-13 RS = 1.12e-2 TRS1 = 1.61e-3 TRS2 = 6.08e-6 CJO = 1.05e-9 TT = 3.84e-8)
.MODEL DBKMOD D (RS = 1.82e-1 TRS1 = 7.50e-3 TRS2 = -4.0e-5)
.MODEL DESD1MOD D (BV = 13.54 TBV1 = 0 TBV2 = 0 RS = 45.5 TRS1 = 0 TRS2 = 0)
.MODEL DESD2MOD D (BV = 11.46 TBV1 = -7.576e-4 TBV2 = -3.0e-6 RS = 0 TRS1 = 0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 0.591e-9 IS = 1e-30 N = 10)
.MODEL MOS1MOD NMOS (VTO = 1.94 KP = 139.2 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.07e-3 TC2 = -3.03e-7)
.MODEL RDSMOD RES (TC1 = 5.38e-3 TC2 = 1.64e-5)
.MODEL RSLVCMOD RES (TC1 = 1.75e-3 TC2 = 3.90e-6)
.MODEL RVTOMOD RES (TC1 = -2.15e-3 TC2 = -5.43e-6)

.MAX TC1 = 1.07e-3 TC2 = 1.64e-5

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**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

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<th>Product Status</th>
<th>Definition</th>
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<td>This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
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