Description
Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRFZ44NL) is available for low-profile applications.

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D$ @ $T_C = 25^\circ C$</td>
<td>49</td>
<td>A</td>
</tr>
<tr>
<td>$I_D$ @ $T_C = 100^\circ C$</td>
<td>35</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DM}$</td>
<td>160</td>
<td>A</td>
</tr>
<tr>
<td>$P_D @ T_A = 25^\circ C$</td>
<td>3.8</td>
<td>W</td>
</tr>
<tr>
<td>$P_D @ T_C = 25^\circ C$</td>
<td>94</td>
<td>W</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>$I_{AR}$</td>
<td>25</td>
<td>A</td>
</tr>
<tr>
<td>$E_{AR}$</td>
<td>9.4</td>
<td>mJ</td>
</tr>
<tr>
<td>$dv/dt$</td>
<td>5.0</td>
<td>V/ns</td>
</tr>
<tr>
<td>$T_J$ Operating Junction and</td>
<td>-55 to +175</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{STG}$ Storage Temperature Range</td>
<td>300 (1.6mm from case)</td>
<td>°C</td>
</tr>
</tbody>
</table>

Thermal Resistance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JIC}$ Junction-to-Case</td>
<td>——</td>
<td>1.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JJA}$ Junction-to-Ambient</td>
<td>——</td>
<td>40</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

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### Source-Drain Ratings and Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>IS</td>
<td>49</td>
<td>49</td>
<td></td>
<td>A</td>
<td>MOSFET symbol showing the integral reverse p-n junction diode.</td>
</tr>
<tr>
<td>ISM</td>
<td>160</td>
<td>160</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDS</td>
<td>1.3</td>
<td>1.3</td>
<td></td>
<td>V</td>
<td>Tj = 25°C, IS = 25A, VGS = 0V</td>
</tr>
<tr>
<td>trr</td>
<td>63</td>
<td>95</td>
<td></td>
<td>ns</td>
<td>Tj = 25°C, IF = 25A</td>
</tr>
<tr>
<td>QrF</td>
<td>170</td>
<td>260</td>
<td></td>
<td>nC</td>
<td>di/dt ≤ 100A/µs</td>
</tr>
<tr>
<td>ItoF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Intrinsic turn-on time is negligible (turn-on is dominated by Ls+Ld).</td>
</tr>
</tbody>
</table>

**Notes:**

1. Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
2. Starting Tj = 25°C, L = 0.48mH
3. ISD ≤ 25A, di/dt ≤ 230A/µs, VDD ≤ VBRIDSS, Tj ≤ 175°C
4. Pulse width ≤ 400µs; duty cycle ≤ 2%.
5. This is a calculated value limited to Tj = 175°C.

**When mounted on 1" square PCB (FR-4 or G-10 Material).**
For recommended footprint and soldering techniques refer to application note #AN-994.
**IRFZ44NS/LPbF**

**Fig 1.** Typical Output Characteristics

**Fig 2.** Typical Output Characteristics

**Fig 3.** Typical Transfer Characteristics

**Fig 4.** Normalized On-Resistance Vs. Temperature

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Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

\[ V_{GS} = 0\, \text{V}, \quad \text{f} = 1\, \text{MHz} \]
\[ C_{iss} = C_{gs} + C_{gd}, \quad C_{ds} \text{ SHORTED} \]

\[ C_{rss} = C_{gd} \]

\[ C_{oss} = C_{ds} + C_{gd} \]

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

\[ I_D = 25\, \text{A} \]
\[ V_{DS} = 44\, \text{V}, \quad V_{DS} = 28\, \text{V} \]

FOR TEST CIRCUIT: SEE FIGURE 13

Fig 7. Typical Source-Drain Diode Forward Voltage

\[ I_{SD}, \, \text{Reverse Drain Current (A)} \]
\[ V_{SD}, \, \text{Source-to-Drain Voltage (V)} \]

\[ T_J = 175\, ^\circ\text{C} \]
\[ T_J = 25\, ^\circ\text{C} \]

\[ V_{GS} = 0\, \text{V} \]

Fig 8. Maximum Safe Operating Area

\[ I_D, \, \text{Drain Current (A)} \]
\[ V_{DS}, \, \text{Drain-to-Source Voltage (V)} \]

\[ T_C = 25\, ^\circ\text{C} \]
\[ T_J = 175\, ^\circ\text{C} \]

Single Pulse

OPERATION IN THIS AREA LIMITED BY R\text{DS(on)}

10\, \mu\text{s} \quad 100\, \mu\text{s} \quad 1\, \text{ms} \quad 10\, \text{ms} \quad 100\, \text{ms} \quad 1\, \text{s}
**Fig 9.** Maximum Drain Current Vs. Case Temperature

**Fig 10a.** Switching Time Test Circuit

**Fig 10b.** Switching Time Waveforms

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Notes:
1. Duty factor $D = t_1 / t_2$
2. Peak $T_{J} = P_{DM} \times Z_{thJC} + T_{C}$
Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Fig 13a. Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit
**IRFZ44NS/LPbF**

**Peak Diode Recovery dv/dt Test Circuit**

![Diagram of the Peak Diode Recovery dv/dt Test Circuit with labels for various components and waveform descriptions.]

1. **Driver Gate Drive**: P.W. Period
   - D = P.W. / Period
   - V_{GS}=10V

2. **D.U.T. \( I_{SD} \) Waveform**: Reverse Recovery Current
   - Body Diode Forward Current
   - \( dV/dt \)

3. **D.U.T. \( V_{DS} \) Waveform**: Diode Recovery dv/dt
   - Body Diode Forward Drop
   - Ripple \( \leq 5\% \)
   - \( I_{SD} \)

4. **Inductor Current**: Re-Applied Voltage

- \( V_{GS} = 5V \) for Logic Level Devices

**Fig14. For N-Channel HEXFETS**

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D²Pak Package Outline
Dimensions are shown in millimeters (inches)

D²Pak Part Marking Information (Lead-Free)

Example:

THIS IS AN IRF530S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead-Free"

OR

INTERNATIONAL RECTIFIER LOGO
PART NUMBER
DATE CODE YEAR 0 = 2000 WEEK 02 LINE L

INTERNATIONAL RECTIFIER LOGO
PART NUMBER
DATE CODE P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)
YEAR 0 = 2000 WEEK 02
A = ASSEMBLY SITE CODE

Dimensions are shown in millimeters (inches)
TO-262 Package Outline

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRLZ34N
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"
Note "P" in assembly line position indicates "Lead-Free"
D²Pak Tape & Reel Information
Dimensions are shown in millimeters (inches)

NOTES:
1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR’s Web site.
Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/