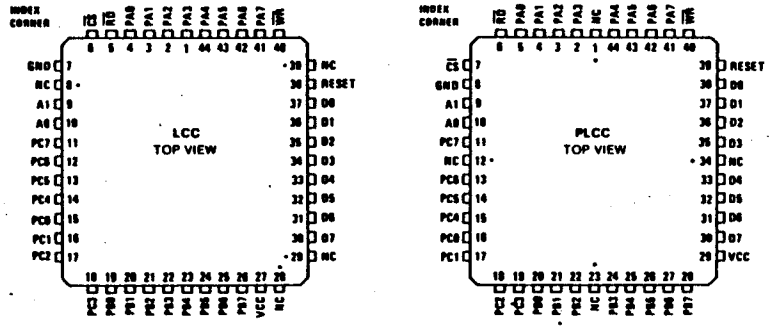
Pin Descriptions

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VCC	26		VCC: the +5V power supply pin. A 0.1μF capacitor between pins 26 and 7 is recommended for decoupling
GND	7		GROUND
D_0-D_7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
WR	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1)
PA_0-PA_7	1-4, 37-40	I/O	PORT A: 8-Bit Input and Output Port. Both bus hold high and bus hold low circuitry are present on this port.
PB_0-PB_7	18-25	I/O	PORT B: 8-Bit input and output port. Bus hold high circuitry is present on this port.
PC_0-PC_7	10-17	I/O	PORT C: 8-Bit input and output port. Bus Hold High circuitry is present on this port.

LCC/PLCC Pinouts



No Connect

Functional Description

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the 82C55A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 82C55A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 82C55A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

82C55A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
1	1	0	1	0	CONTROL WORD → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
X	X	1	1	0	DATA BUS → 3-STATE

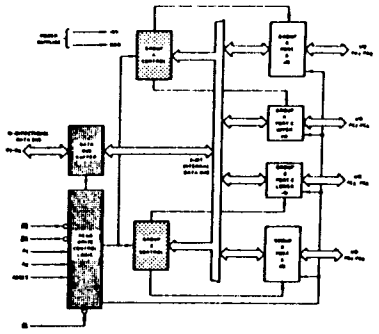


Figure 1
82C55A Block Diagram
Data Bus Buffer, Read/Write, Group A & B
Control Logic Functions

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the 82C55A will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400 μA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)

Control Group B – Port B and Port C lower (C3-C0)

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A. See Figure 2a.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2b.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. See Figure 2b.

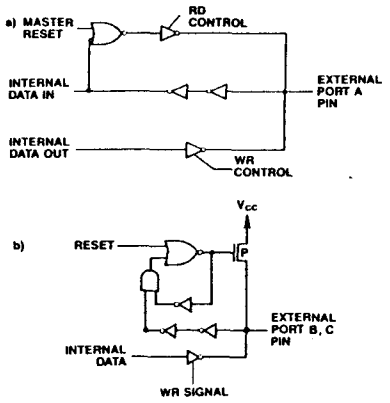


Figure 2
Port A & B, Port C Bus-hold Configuration

Operational Description

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown resistors in all-CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

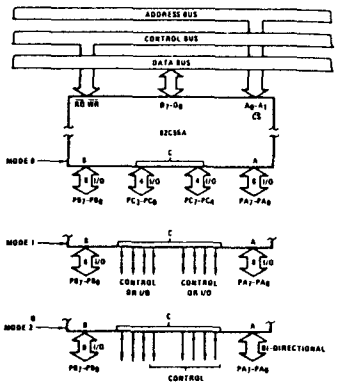


Figure 3
Basic Mode Definitions and Bus Interface

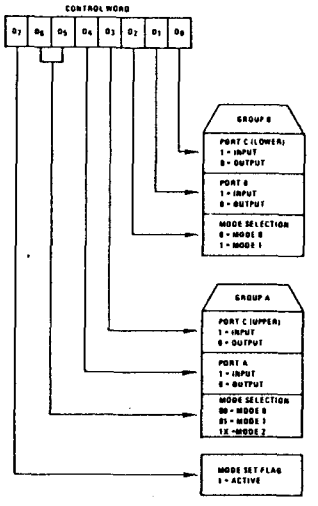


Figure 4
Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

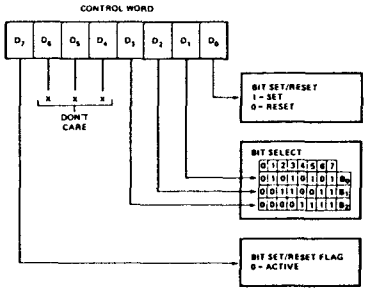


Figure 5
Bit Set/Reset Format

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) – INTE is SET – Interrupt enable
(BIT-RESET) – INTE is RESET – Interrupt disable.

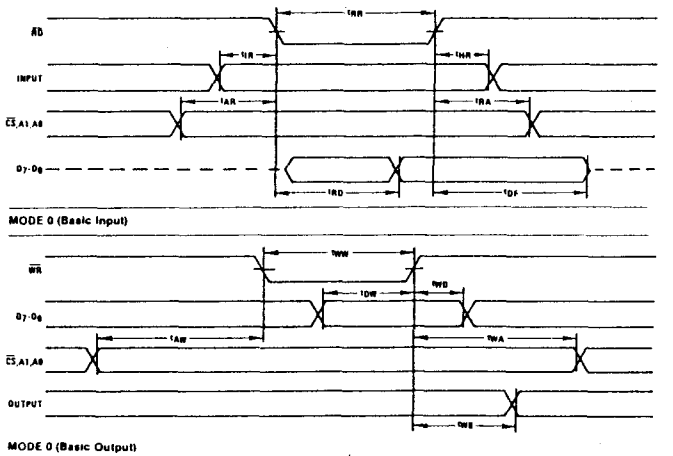
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

Mode 0 Basic Functional Definitions:

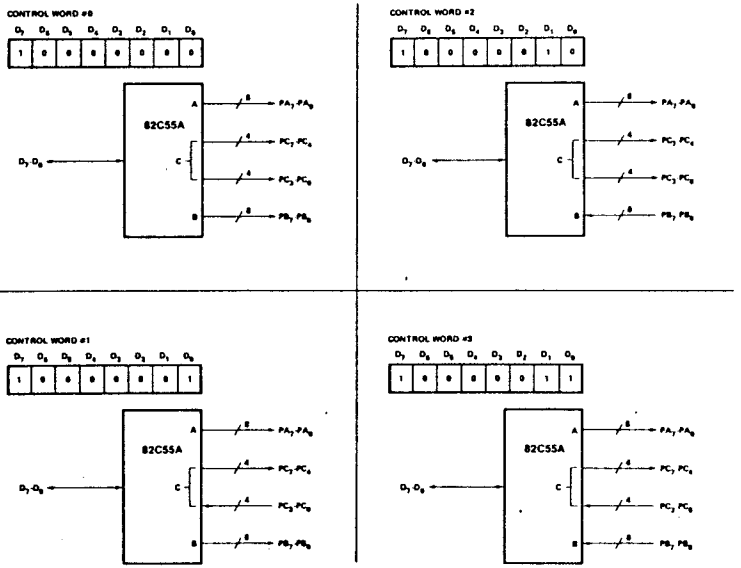
- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible

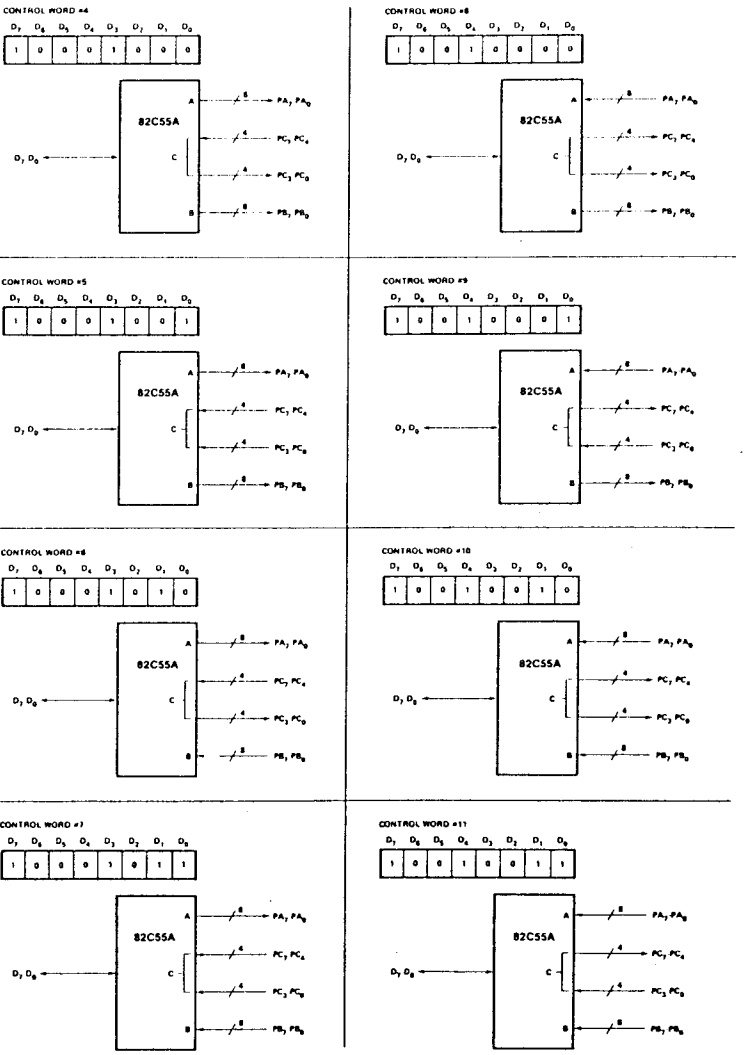


MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations





Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	◄—►	
PA_1	IN	OUT	IN	OUT	◄—►	
PA_2	IN	OUT	IN	OUT	◄—►	
PA_3	IN	OUT	IN	OUT	◄—►	
PA_4	IN	OUT	IN	OUT	◄—►	
PA_5	IN	OUT	IN	OUT	◄—►	
PA_6	IN	OUT	IN	OUT	◄—►	
PA_7	IN	OUT	IN	OUT	◄—►	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations:

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

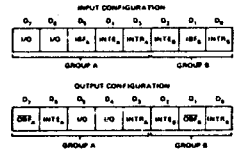


Figure 15. MODE 1 Status Word Format

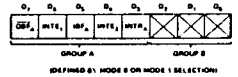


Figure 16. MODE 2 Status Word Format

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and OBF) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

Interrupt Enable Flag*	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
INTE A2	PC4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

Figure 17
Interrupt Enable Flags in Modes 1 and 2

Current Drive Capability:

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

APPLICATIONS OF THE 82C55A

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly "fit" the application. Figures 18 through 24 present a few examples of typical applications of the 82C55A.

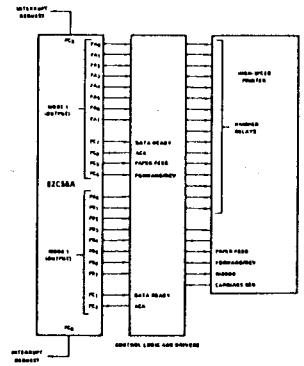


Figure 18. Printer Interface

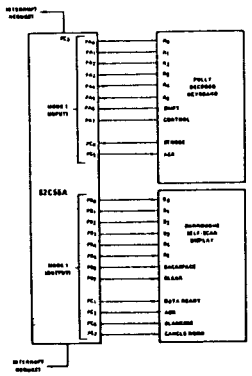


Figure 19. Keyboard and Display Interface

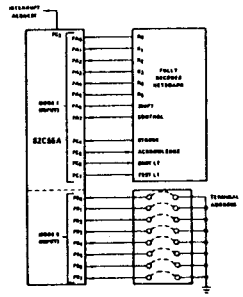


Figure 20. Keyboard and Terminal Address Interface

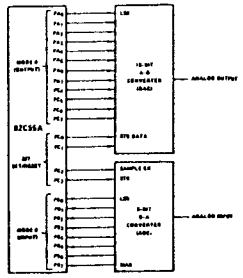


Figure 21. Digital to Analog, Analog to Digital

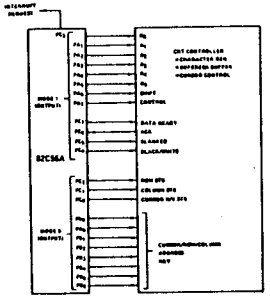


Figure 22. Basic CRT Controller Interface

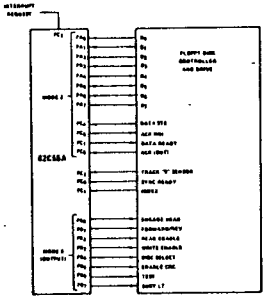


Figure 23. Basic Floppy Disc Interface

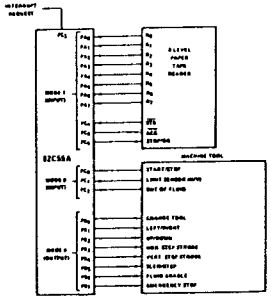


Figure 24. Machine Tool Controller Interface

Absolute Maximum Ratings

Supply Voltage	+8.0 Volts
Input, Output or I/O Voltage Applied	GND -0.5V to VCC +0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1 Watt
θ_{jc}	22°C/W (CERDIP Package), 27°C/W (LCC Package)
θ_{ja}	55°C/W (CERDIP Package), 60°C/W (LCC Package)
Gate Count	1,000 Gates
Junction Temperature	+150°C
Lead Temperature (Soldering, Ten Seconds)	+260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.5V to +5.5V
Operating Temperature Range	
C82C55A	0°C to +70°C
I82C55A	-40°C to +85°C
M82C55A	-55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ± 10%; T_A = 0°C to +70°C (C82C55A); T_A = -40°C to +85°C (I82C55A); T_A = -55°C to +125°C (M82C55A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	I82C55A, C82C55A, M82C55A
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Logical One Output Voltage	3.0 VCC -0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Logical Zero Output Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	1.0	μA	VIN = VCC OR GND, DIP Pins: 5, 6, 8, 9, 35, 36
IO	I/O Pin Leakage Current	-10.0	10.0	μA	VO = VCC or GND DIP Pins: 27-34
IBHH	Bus Hold High Current	-50	-400	μA	VO = 3.0V Ports A, B, C
IBHL	Bus Hold Low Current	+50	+400	μA	VO = 1.0V PORT A ONLY
IDAR	Darlington Drive Current	-2.0	Note 1	mA	PORTS A, B, C Test Condition 3
ICCSB	Standby Power Supply Current		10	μA	VCC = 5.5V, VIN = VCC or GND Outputs Open
ICCOP	Operating Power Supply Current		1	mA/MHz	T_A = +25°C, VCC = 5.0V, Typical (See Note 2)

NOTES: 1. No internal current limiting exists on Port Outputs. A resistor must be added externally to limit the current.
2. ICCOP = 1mA/MHz of Peripheral Read/Write cycle time. (Example: 1.0μs I/O Read/Write cycle time = 1mA).

Capacitance

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND.

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	5	pF	FREQ = 1MHz Unmeasured pins returned to GND
$C_{I/O}$	I/O Capacitance	20	pF	

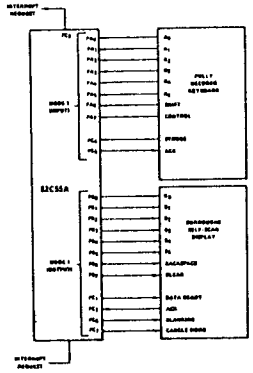


Figure 19. Keyboard and Display Interface

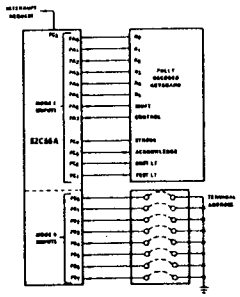


Figure 20. Keyboard and Terminal Address Interface

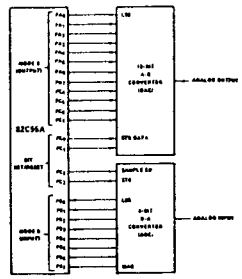


Figure 21. Digital to Analog, Analog to Digital

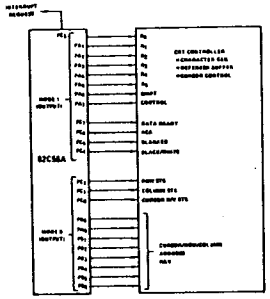


Figure 22. Basic CRT Controller Interface

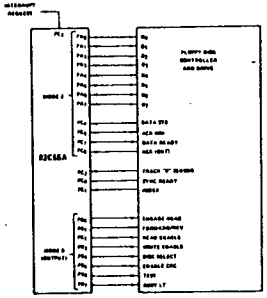


Figure 23. Basic Floppy Disc Interface

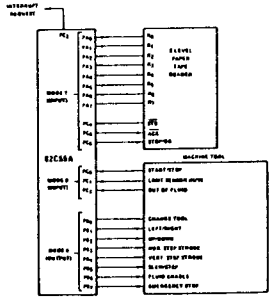


Figure 24. Machine Tool Controller Interface

Absolute Maximum Ratings

Supply Voltage	+8.0 Volts
Input, Output or I/O Voltage Applied	GND -0.5V to VCC +0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1 Watt
θ_{jc}	22°C/W (CERDIP Package), 27°C/W (LCC Package)
θ_{ja}	55°C/W (CERDIP Package), 60°C/W (LCC Package)
Gate Count	1,000 Gates
Junction Temperature	+150°C
Lead Temperature (Soldering, Ten Seconds)	+260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.5V to +5.5V
Operating Temperature Range	
C82C55A	0°C to +70°C
I82C55A	-40°C to +85°C
M82C55A	-55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ± 10%; T_A = 0°C to +70°C (C82C55A); T_A = -40°C to +85°C (I82C55A); T_A = -55°C to +125°C (M82C55A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	I82C55A, C82C55A, M82C55A
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Logical One Output Voltage	3.0 VCC -0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Logical Zero Output Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	1.0	μA	VIN = VCC OR GND, DIP Pins: 5, 6, 8, 9, 35, 36
IO	I/O Pin Leakage Current	-10.0	10.0	μA	VO = VCC or GND DIP Pins: 27-34
IBHH	Bus Hold High Current	-50	-400	μA	VO = 3.0V Ports A, B, C
IBHL	Bus Hold Low Current	+50	+400	μA	VO = 1.0V PORT A ONLY
IDAR	Darlington Drive Current	-2.0	Note 1	mA	PORTS A, B, C Test Condition 3
ICCSB	Standby Power Supply Current		10	μA	VCC = 5.5V, VIN = VCC or GND Outputs Open
ICCOP	Operating Power Supply Current		1	mA/MHz	T_A = +25°C, VCC = 5.0V, Typical (See Note 2)

NOTES: 1. No internal current limiting exists on Port Outputs. A resistor must be added externally to limit the current.
2. ICCOP = 1mA/MHz of Peripheral Read/Write cycle time. (Example: 1.0μs I/O Read/Write cycle time = 1mA).

Capacitance

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND.

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	5	pF	FREQ = 1MHz Unmeasured pins returned to GND
$C_{I/O}$	I/O Capacitance	20	pF	

A.C. Electrical Specifications

VCC = +5V ± 10%, GND = 0V; T_A = −55°C to +125°C (M82C55A) (M82C55A-5)
VCC = +5V ± 10%, GND = 0V; T_A = −40°C to +85°C (I82C55A) (I82C55A-5)
VCC = +5V ± 10%, GND = 0V; T_A = 0°C to +70°C (C82C55A) (C82C55A-5)

Bus Parameters

READ

SYMBOL	PARAMETER	82C55A MIN	82C55A MAX	82C55A-5 MIN	82C55A-5 MAX	UNITS	TEST CONDITIONS
tAR	Address Stable Before READ	0		0		ns	
tRA	Address Stable After READ	0		0		ns	
tRR	READ Pulse Width	150		250		ns	
tRD	Data Valid From READ		120		200	ns	1
tDF	Data Float After READ	10	75	10	75	ns	2
tRV	Time Between READs and/or WRITEs	300		300		ns	

WRITE

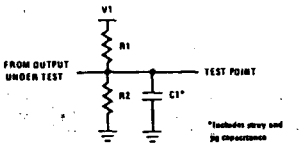
SYMBOL	PARAMETER	82C55A MIN	82C55A MAX	82C55A-5 MIN	82C55A-5 MAX	UNITS	TEST CONDITIONS
tAW	Address Stable Before WRITE	0		0		ns	
tWA	Address Stable After WRITE	20		20		ns	
tWW	WRITE Pulse Width	100		100		ns	
tDW	Data Valid to WRITE High	100		100		ns	
tWD	Data Valid After WRITE High	30		30		ns	

OTHER TIMINGS

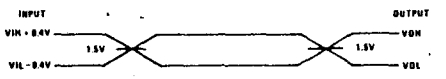
SYMBOL	PARAMETER	82C55A MIN	82C55A MAX	82C55A-5 MIN	82C55A-5 MAX	UNITS	TEST CONDITIONS
tWB	WR = 1 to Output		350		350	ns	1
tIR	Peripheral Data Before RD	0		0		ns	
tHR	Peripheral Data After RD	0		0		ns	
tAK	ACK Pulse Width	200		200		ns	
tST	STB Pulse Width	100		100		ns	
tPS	Per. Data Before STB High	20		20		ns	
tPH	Per. Data After STB High	50		50		ns	
tAD	ACK = 0 to Output		175		175	ns	1
tKD	ACK = 1 to Output Float	20	250	20	250	ns	2
tWOB	WR = 1 to OBF = 0		150		150	ns	1
tAOB	ACK = 0 to OBF = 1		150		150	ns	1
tSIB	STB = 0 to IBF = 1		150		150	ns	1
tRIB	RD = 1 to IBF = 0		150		150	ns	1
tRIT	RD = 0 to INTR = 0		200		200	ns	1
tSIT	STB = 1 to INTR = 1		150		150	ns	1
tAIT	ACK = 1 to INTR = 1		150		150	ns	1
tWIT	WR = 0 to INTR = 0		200		200	ns	1
tRES	Reset Pulse Width	500		500		ns	see note 1

Note 1. Period of initial Reset pulse after power-on must be at least 50 μsec. Subsequent Reset pulses may be 500ns minimum.

A. C. Test Circuit



A.C. Testing Input, Output Waveforms



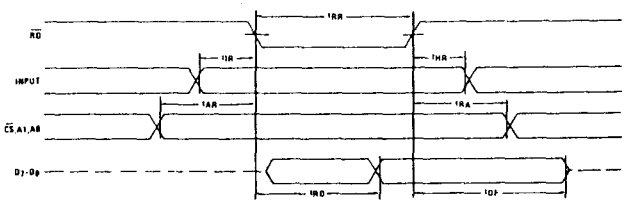
A.C. Testing: All parameters tested as per test circuits. Input rise and fall times are driven at 1ns/V.

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	150 pf
2	5.0V	2KΩ	1.7KΩ	50 pf
3	1.5V	750Ω	OPEN	OPEN

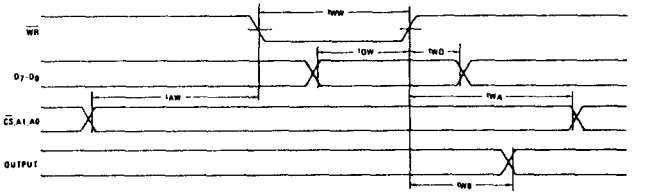
TEST CONDITION DEFINITION TABLE

Waveforms

MODE 0 (BASIC INPUT)



MODE 0 (BASIC OUTPUT)



MODE 1 (STROBED INPUT)