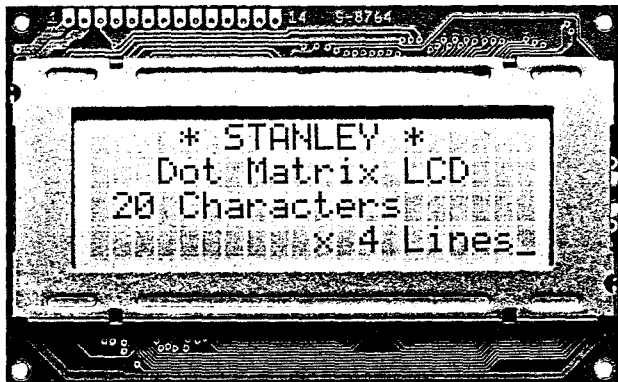
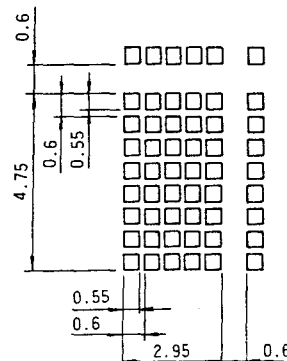


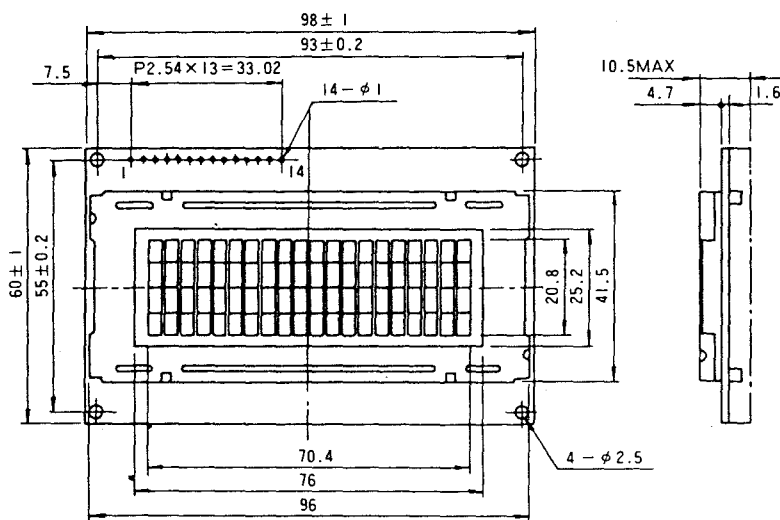
GMD2040A 20 Characters × 4 Lines 1/16 Duty



● Display Pattern



● Module Dimensions (Reflective)



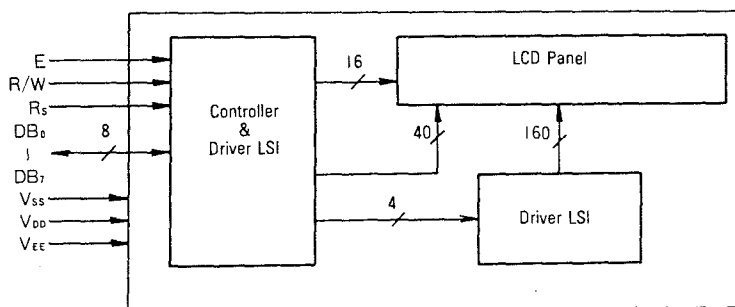
Unit: mm

● Interface Pin Function

Pin No.	Symbol	Level	Function	
1	V <sub>SS</sub>	—	Power Supply	
2	V <sub>DD</sub>	—		OV (GND)
3	V <sub>EE</sub>	—		+5V for Liquid Crystal driving
4	R <sub>s</sub>	H/L	Register select H: Data Input L: Instruction Input	
5	R/W	H/L	H: Data Read (Module → MPU) L: Data Write (Module ← MPU)	
6	E	H, H ← L	Operation start signal for data read/write	
7	DB0	H/L	Lower order 4 lines data bus with bidirectional three-state. Used for data transfer between the MPU and the module. These four are not used during 4-bit operation.	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L	Higher order 4 lines data bus with bidirectional three-state. Used for data transfer between the MPU and the module. DB 7 can be used as a BUSY flag.	
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
*15	A (LED+)	—	Supply Voltage for LED Backlighting	
*16	K (LED-)	—	OV (GND)	

Note) \* marked pins are only for LED backlighting type.

● Block Diagram



● DD RAM Address

	1	2	3	4	5	6	.....	15	16	17	18	19	20
Line 1	00	01	02	03	04	05		0E	0F	10	11	12	13
Line 2	40	41	42	43	44	45		4E	4F	50	51	52	53
Line 3	14	15	16	17	18	19		22	23	24	25	26	27
Line 4	54	55	56	57	58	59		62	63	64	65	66	67

RAM area: 00 H ~ 27 H & 40 H ~ 67 H

# Characteristics

## Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Logic Circuit Supply Voltage	V <sub>DD</sub> -V <sub>SS</sub>	0	7.0 (6.5) ※1	V
LCD Driver Circuit Supply Voltage	V <sub>DD</sub> -V <sub>EE</sub>	0	13.5 (6.5) ※1	V
Input Voltage	V <sub>I</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V
Operating Temperature	T <sub>op</sub>	0	50	°C
Storage Temperature	T <sub>stg</sub>	-20	70	°C

Note) ※ 1: The figures in ( ) are applicable to GMD1640A, GMD2040A and GMD4020E Series.

## Electrical Characteristics

V<sub>DD</sub>=5.0±0.25V Ta=0~+50°C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input "High" Voltage	V <sub>IH</sub>	—	2.2	—	V <sub>DD</sub>	V
Input "Low" Voltage	V <sub>IL</sub>	—	0	—	0.6	V
Output "High" Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -0.205mA	2.4	—	—	V
Output "Low" Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.2mA	—	—	0.4	V
Clock frequency	f <sub>osc</sub>	—	190	270	350	KHz

## Optical Characteristics

Ta = +25°C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage for LCD «1/16 Duty»	V <sub>DD</sub> -V <sub>EE</sub>	Ta = 50°C	—	3.7	—	V
		Ta = 25°C	—	4.4	—	V
		Ta = 0°C	—	4.9	—	V
Contrast ratio (Fig. 1)	K	φ = 20° θ = 0°	3	—	—	—
Viewing Angle (Fig. 2)	φ <sub>2</sub> -φ <sub>1</sub>	θ = 0° K ≧ 1.4	20	—	—	Degree
	θ	φ = 20° K = 1.4	±30	—	—	Degree
Response time (Fig. 3)	rise	φ = 20° θ = 0°	—	150	250	m sec
	fall	φ = 20° θ = 0°	—	150	250	m sec

Note) • This specifications is applicable to TN positive type LCD. Please ask us when you need the specifications of other LCD except TN positive type shown in the above list.  
• Measured on LCD only. If there is any heat source (LED, CFL, etc.) exist around LCD the temperature increase should be taken into consideration.

Fig. 1 Definition of contrast ratio (K)

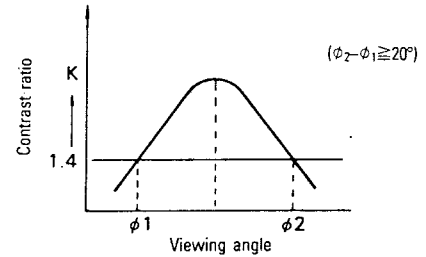
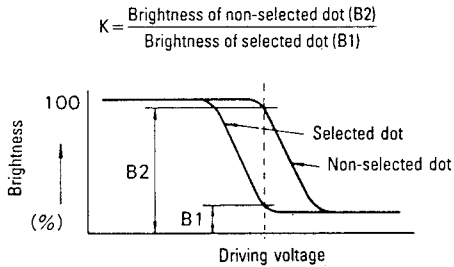


Fig. 2 Definition of viewing angle φ<sub>2</sub>-φ<sub>1</sub>, θ

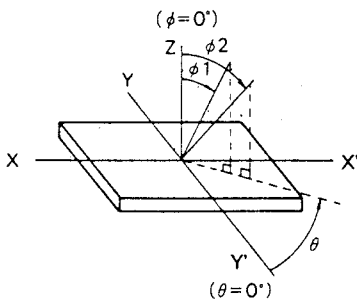
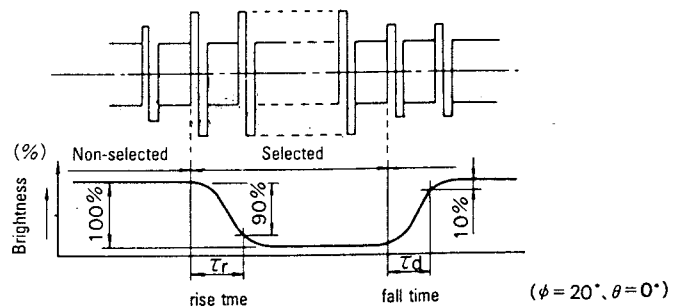


Fig. 3 Definition of response time



# Characteristics of Control LSI

## ■ Timing Chart (interface timing)

### ■ Data Write

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Enable cycle time	tcyc	Fig. 4	1.0	—	—	μ sec
Enable pulse width	PwEH	Fig. 4	450	—	—	n sec
Enable rise/fall time	t <sub>er</sub> /t <sub>ed</sub>	Fig. 4	—	—	25	n sec
Address set up time	t <sub>as</sub>	Fig. 4	140	—	—	n sec
Address hold time	t <sub>ah</sub>	Fig. 4	10	—	—	n sec
Data set up time	t <sub>ds</sub>	Fig. 4	195	—	—	n sec
Hold time	t <sub>h</sub>	Fig. 4	10	—	—	n sec

### ■ Data Read

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Enable cycle time	tcyc	Fig. 5	1.0	—	—	μ sec
Enable pulse width	PwEH	Fig. 5	450	—	—	n sec
Enable rise/fall time	t <sub>er</sub> /t <sub>ed</sub>	Fig. 5	—	—	25	n sec
Address set up time	t <sub>as</sub>	Fig. 5	140	—	—	n sec
Address hold time	t <sub>ah</sub>	Fig. 5	10	—	—	n sec
Data delay time	t <sub>DDR</sub>	Fig. 5	—	—	320	n sec
Data hold time	t <sub>DHR</sub>	Fig. 5	20	—	—	n sec

Fig. 4 Data Write from MPU to Module

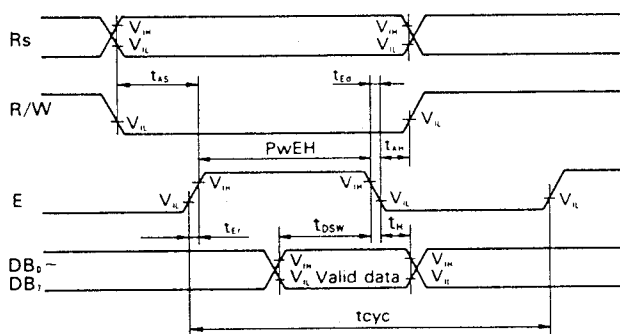
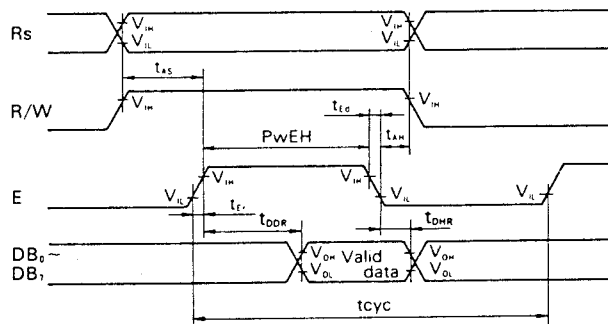
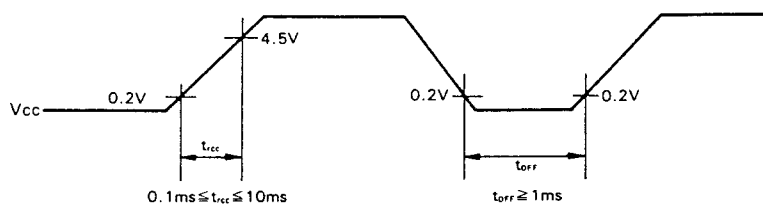


Fig. 5 Data Read from Module to MPU



## ■ Reset Function

The LCD Module automatically performs initialization (reset) when power is turned on (using internal reset circuit). However, since initialization may not be performed completely depending on the rise time of the power supply when it is turned on, pay attention to the following time-relationship.



Note) Since the internal reset circuit will not operate normally unless the preceding conditions are met, initialize by instruction.

## Instructions

Instruction	Code											Description	Execution time (Max) (when fosc is 250kHz)	
	Rs	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0				
Clear display	0	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DD RAM address 0 in address counter.	1.64m sec	
Return home	0	0	0	0	0	0	0	0	0	1	*	sets DD RAM address 0 in address counter. Also returns display being shifted to original position. DD RAM counters remain unchanged.	1.64m sec	
Entry mode set	0	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40μ sec	
Display ON/OFF control	0	0	0	0	0	0	0	1	D	C	B	sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40μ sec	
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	*	*		moves cursor and shifts display without changing DD RAM contents.	40μ sec	
Function set	0	0	0	0	1	DL	N	F	*	*		sets interface data length (DL), number of display lines (N) and character font (F).	40μ sec	
Set CG RAM address	0	0	0	1	ACG								sets CG RAM address. CG RAM data are sent and received after this setting.	40μ sec
Set DD RAM address	0	0	1	ADD								sets DD RAM address. DD RAM data are sent and received after this setting.	40μ sec	
Read busy flag & address	0	1	BF	AC								reads busy flag (BF) indicating internal operation is being performed and reads address counter contents.	1μ sec	
Write data to CG or DD RAM	1	0	Write Data								writes data into DD RAM or CG RAM	40μ sec		
Read data from CG or DD RAM	1	1	Read Data								reads data from DD RAM or CG RAM	40μ sec		
I/D = 1: Increment I/D = 0: Decrement S = 1: Accompanies display shift S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8 bits, DL = 0: 4 bits N = 1: 2 lines, N = 0: 1 line. *Note 1) F = 1: 5 × 10 dots, F = 0: 5 × 7 dots BF = 1: Internally operating BF = 0: Can accept instruction											DD RAM: Display data RAM CG RAM: Character generator RAM ACG : CG RAM address ADD : DD RAM address Corresponds to cursor address AC : Address counter used for both CG and DD RAM address * : Invalidity		Execution time changes when frequency changes.  (Example) When fosc is 270kHz: $40\mu\text{ sec} \times \frac{250}{270} = 37\mu\text{ sec}$	

\*Note 1) In the case of GMD 1610F, GMD1610FL\* (16 character 1 line 1/16 duty), set N = 1.

# Operation Example

## ■ 8-bit operation, 2 line display

No.	Instruction (Rs R/W DB <sub>7</sub> ~DB <sub>0</sub> )	Display	Operation
1	Power supply ON (Initialized by the internal reset circuit)		Initialized. No display appears.
2	Function set (00001110**)		Set 8 bit operation and select 2-line display and 5 × 7 dot character font.
3	Display ON/OFF control (0000001110)		Turn on display and cursor. Entire display is in space mode because of initialization.
4	Entry mode set (0000000110)		Set mode to increment the address by one and to shift the cursor to the right, at the time of write, to the CG/DD RAM. Display is not shifted.
5	Write data to CG RAM/DD RAM (1001010011)	S	Write "S". The DD RAM has already been selected by initialization. The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM/DD RAM (1001010100)	ST	Write "T".
⋮	⋮	⋮	⋮
11	Write data to CG RAM/DD RAM (1001011001)	STANLEY	Write "Y".
12	Set DD RAM address (0011000000)	STANLEY	Set RAM address so that the cursor is positioned at the head of the 2nd. line.
13	Write data to CG RAM/DD RAM (1000111000)	STANLEY 8	Write "8".
⋮	⋮	⋮	⋮
20	Write data to CG RAM/DD RAM (1001000100)	STANLEY 8 bitMOD	Write "D".
21	Write data to CG RAM/DD RAM (1001000101)	STANLEY 8 bitMODE	Write "E".


## ■ In the case of 4-bit operation

When power is turned on, 8-bit operation is automatically selected, so the program must be set functions prior to 4-bit operation. One operation is completed in two accesses of 4-bit operations.

Note: For 2 lines display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written.

# Correspondence between Character Code and Character Pattern

		0	2	3	4	5	6	7	A	B	C	D	E	F
	Upper 4bit Lower 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0	xxxx0000 CG RAM (1)		0	1	2	3	4	5	6	7	8	9	A	B
1	xxxx0001 (2)	!	1	2	3	4	5	6	7	8	9	A	B	
2	xxxx0010 (3)	!	2	3	4	5	6	7	8	9	A	B		
3	xxxx0011 (4)	!	3	4	5	6	7	8	9	A	B			
4	xxxx0100 (5)	!	4	5	6	7	8	9	A	B				
5	xxxx0101 (6)	!	5	6	7	8	9	A	B					
6	xxxx0110 (7)	!	6	7	8	9	A	B						
7	xxxx0111 (8)	!	7	8	9	A	B							
8	xxxx1000 (1)	!	8	9	A	B								
9	xxxx1001 (2)	!	9	A	B									
A	xxxx1010 (3)	!	A	B										
B	xxxx1011 (4)	!	B											
C	xxxx1100 (5)	!	C											
D	xxxx1101 (6)	!	D											
E	xxxx1110 (7)	!	E											
F	xxxx1111 (8)	!	F											

(e.g. HEX 2F CHAR>DISPLAY yields )

**Character Generator RAM (CG RAM)**  
 The character generator RAM is the RAM with which the user can rewrite character patterns by program. With 5 x 7 dots, 8 types of character patterns can be written. Write the character codes in the left columns of above table. For details, please consult with Stanley.