

## Summary

The following software describes how to use peripheral port A (PPA) for PWM or as a DAC.

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$\backslash$	* * * * * * * * * *	This code is provided to customers of the QED Board	* * * * * * * * * *
$\setminus$	* * * * * * * * * *	for use with the QED Board Software Development	* * * * * * * * * *
$\setminus$	* * * * * * * * * *	environment. The provision of this code is governed	* * * * * * * * * *
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_\ t	the apparent	pulse width modulates bits of peripheral port A (PPA)	
\     \     \ s   \ 2   \ 2   \ 2	bits of PPA levels are p smooths the The PWM algo averaging ti good for ana which the ap	pseudo-period of the PWM waveform is as short as poss ution of one part in 256. This enables, among other f to be low pass filtered to create 8-bit DAC channels. roduced. Downstream of the digital output a low pass PWM signal into an average value with a small residual rithm is optimal in the respect that it requires the l	sible, and Functions, s filter ripple. east erty makes it gnals in sible. This

 $\land$  that is as good an approximation of the true duty cycle as it can be. The  $\setminus$  error in duty cycle (or resolution if used as a DAC) is limited to less than  $\setminus 1/(2*n)$  where n is the number of consecutive updates of the port bits up to  $\$  n=256, the full period. For n=256 the duty cycle error is zero because the  $\$  duty cycles are produced exactly with a period of 256 updates. / \* \* \* \* \* \* \* \* \* \* Under the Hood: How It Works \  $\setminus$  For a detailed description of the PWM algorithm used see the Mosaic Industries  $\setminus$  QED Application Note "MI-AP-056: A PWM Algorithm with Optimal Averaging \ Properties".  $\setminus$  An interrupt service routine services PPA every t seconds, where t can  $\$  be adjusted from a minimum of about 2 msec (it takes 1.1 msec to service all  $\$  the PPA bits) to as much as 131 msec. If used as a DAC downstream filtering If used as a DAC downstream filtering If the filtering time constant, Tau, is less than 256\*t \ is required. \ there is significant ripple. For every doubling of Tau beyond Tau=t \ the ripple is reduced a factor of two and a bit or resolution is gained, up  $\$  to Tau=256\*t. Beyond that the ripple continues to decrease but no more  $\setminus$  resolution is gained, and the settling time is needlessly lengthened.  $\setminus$  For example, with an interrupt service time set to 2 msec and a downstream \ filter time constant of 0.5 sec or greater the filter time is 256 times the \ minimum, and the DAC resolution is a full 8-bits. This code sets the \ interrupt service time to a default value of 2 msec; I recommend that a downstream filtering time constant of 0.5 seconds be used. / / How to Use It / Download this text file. / 1. ١ Configure PPA for output using TRUE flag INIT. PIA The TRUE initializes PPA as output. \ 2. ١ \ \ flag = true indicates that upper PPC is output. Choose upper PPC to be input or output as you need. \

Execute ١ **6**. / Start. PPA. PWM to install the interrupt service routine and start periodic updates of No PWM waveforms are generated until you specify duty the PPA bits. cycles using >PPA. PWM 7. Execute >PPA. PWM  $(\mathbf{u} \mathbf{n} - -)$ to send a PWM duty cycle to any PPA output pin. This top level word takes as input an 8-bit unsigned value, u, as the PWM duty cycle and the PPA pin number, n, where  $0 \le n \le 7$ . Other output pins are unaffected. Values of u from 0 to 256 are allowed, with 256 indicating a continuously ON condition. The duty cycle is given by D. C. = u/256. The time between updates of the output pins is determined by the value of PERIOD, which holds the time as the number of 2 usec ticks of the TCNT clock. If you are filtering the PWM outputs for digital to analog conversion 8. then use the word >PPA. DAC (u n - -)instead of >PPA. PWM ( u\n -- ) This word will cause the PWM signal to over or undershoot appropriately whenever there is a change of duty cycle to compensate for the filter delay so that the DAC output is updated as rapidly as possible. For For this to work optimally the filter time constant should be 256 times the update interval. Also, you must install an analog filter with a time constant of 0.5 sec (256 times the update interval of 2 msec) or more on the PPA pin. Α 50 Kohm resistor and 10 uF capacitor will provide the proper time constant. If a low impedance output is needed the filter should be followed by an op-amp voltage follower, or the filter and op-amp may be combined as an active filter. To stop the PWM waveforms execute 9. Stop. PPA. PWM and the interrupt service routine will stop. The PPA output pins that had been used will be left set to zero, except for any that had been set ١ fully on (high) by sending a duty cycle of 256. They will be left high. \  $\mathbf{N}$ The following are descriptions of all the user words:  $\land$  Start. PPA. PWM ( -- ) \ Starts up the periodic interrupt service of the PPA bits but doesn't \ actually modify any bits until >PPA. PWM is executed.

**Stop. PPA. PWM** ( - - )  $\hat{\}$  Stops the interrupt service of the PPA bits, leaving the bits that had  $\land$  been PWMing set to the zero, and not affecting other bits. Start.PPA.PWM ( -- )  $\setminus$  Restarts up the PIA's periodic interrupt service returning the PIA bits  $\setminus$  that had been PWMing before Stop.PPA.PWM had been executed back to their  $\land$  ReStart. PPA. PWM  $\setminus$  PWM action.  $\land$  >PPA. PWM (  $u \land n - -$  )  $\setminus$  u is an unsigned 8-bit PWM value to send to PPA and 0 <= n <= 7 is  $\$  the PPA output bit number. Values of u from 0 to 256 are allowed, with 256  $\$  indicating a continuously ON condition. The time between updates of the  $\$  output pins is determined by the value of PERIOD, which holds the time  $\$  as the number of 2 usec ticks of the TCNT clock.  $\land >$ **PERIOD** (u -- )  $\setminus$  u is and unsigned integer representing the number of 2 microsecond clock  $\setminus$  ticks of TCNT between updates of the PWMed PPA outputs. A period of 2  $\land$  milliseconds would require u = 1000. PERIODs less than 2 msec are not  $\$  recommended as the servicing of PPA takes about 1.1 msec. \ If the PERIOD is too small interrupts will be missed and full TCNT \ rollover periods of 131 msec will be inserted as delays into the interrupt \ servicing. The PERIOD is initialized to 2 msec by Start. PPA. PWM, and can  $\setminus$  be changed thereafter by >PERIOD. \ \*\*\*\*\*\* \ \*\*\*\*\*\* The Code \*\*\*\*\*\*\* ANEW < PPA. PWM> 6 WIDTH !  $\setminus$  Holds the period between interrups as the number of VARIABLE PERIOD  $\setminus$  2 microsecond ticks of TCNT. A value of 1000  $\setminus$  corresponds to 2 msec. HEX 801A REGISTER: TOC3 8020 REGISTER: TCTL1 8022 REGISTER: TMSK1 8023 REGISTER: TFLG1 20 CONSTANT OC3. MASK 10 CONSTANT OC3. LEVEL. MASK CONSTANT OC3. MODE. MASK 20 **DECIMAL** 

∖un: ∖as	ly a single byte is used for the 8-bit signed value to be written to the output pin a PWM signal for values from 0 to 255. r use as a running average PWM for this channel.					
\ Create a single structure containing all eight DAC channel records:						
Structure. Begin: Info. for. PPA. PWM 8 PPA. Record * RESERVED Structure. End						
$\setminus$ Now we instantiate (reserve space for) the PIA.DAC.Info structure in variable $\setminus$ space:						
Info.for.PPA.PWM V.INSTANCE: PPA.PWM.Data						
Variable PPA.Bits.Used \ a byte mask with bits set corresponding to PPA \ output bits used for PVM. Other bits are unaffected.						
<ul> <li>If we were not to use the above data structure we would need the following</li> <li>two variables for each PWM channel. They are shown here only for clarity.</li> <li>The variable Average. PWM must directly follow the variable Target. PWM</li> <li>in memory.</li> </ul>						
\ or	lds the target PWM as an 8-bit number in the high der byte. The contents of the low order byte are relevant. Fetch or store to this variable using C@ d C!.					
\ av \ Ta: \ up \ qu: \ re: \ or	ed internally by the algorithm; holds a running erage PWM To update the PWM immediately set both rget. PWM and Average. PWM to the new value. To date the 256-bit long integral of the output most ickly do not modify Average. PWM when Target. PWM is set. The Average. PWM is set by setting its high der byte to the desired PWM (0-255) and setting s low order byte to 255.					
\ The following is a high level version of the corresponding assembly language \ routine. It is provided here for documentary purposes only:						

?Update. PWM ( xaddr -- Flag ) \ This word implements as PWM routine that optimally averages.
\ xaddr is the address of Target. PWM and xaddr+2 is the address of \ \ \ Average. PWM, both as 16-bit unsigned integers.  $\setminus$  Flag is the bit to be outputted, either true for high or false for low. \ ackslash Each time Update. PWM is called Flag is set to either true or false \  $\setminus$  to maintain the proper average value for the PWM output. ١ ١ [ BASE @ HEX ] Ń XDUP 2 XN+ / Locals{ x&Average.addr x&Target.addr } 1 x&Target.addr @ FF00 AND x&Average.addr @ U> \ IF \ \ x&Average. addr @ x&Average. addr C@ - 00FF + x&Average. addr ! TRUE ١ ELSE x&Average. addr @ x&Average. addr C@ -١ x&Average. addr ! FALSE ١ ١ ENDI F [ BASE ! ] \ The following code is an assembly language version of the above high level  $\land$  routine. ?Update.PWM ( xaddr -- Flag )  $\setminus$  xaddr is the address of Target.PWM as a single byte and xaddr+1 is the CODE ?Update. PWM  $\land$  address of Average. PWM as a 16-bit unsigned integer. (In the high level \ example above they were both 16-bit integers. In this version the Target
\ value is assumed to take only one byte in memory. )
\ Flag is the bit to be outputted, true indicates one or high.
\ Each time ?Update. PWM is called Flag is set to either true or false  $\setminus$  to maintain the proper average value for the PWM output. BASE @ HEX 02 IND, Y LDD \ Get the Target. PWM address 01 IMM ADDD  $\land$  and increment by 1 and push it on the stack DEY DEY OO IND, Y STD O2 IND, Y LDD DEY DEY OO IND, Y STD  $\land$  as the Average. PWM address.  $\setminus$  Fetch and push the page too. 02 IND, Y LDD \ Then XDUP the Average. PWM xaddress DEY DEY OO IND, Y STD 02 IND, Y LDD DEY DEY OO IND, Y STD CALL @  $\land$  @ Average. PWM and push it \ get Average. PWM/256 00 IND, Y LDAB CLRA DEY DEY OO IND, Y STD \ push Average. PWM/256 \ replace Average. PWM/256 on tos with \ Average. PWM - Average. PWM/256 02 IND, Y LDD 00 IND, Y SUBD 00 IND, Y STD D \ put Target address on tos D \ put Target page on tos \ C@ Target. PWM and push it OA IND, Y LDD DEY DEY OO IND, Y STD OA IND, Y LDD DEY DEY OO IND, Y STD CALL C@ 01 IND, Y LDAA  $\setminus$  get target from stack into high byte of D CLRB  $\setminus$  zero out the low order byte 04 IND, Y CPD \ Target. PWM - Average. PWM

HI	IF,	TRUE IMM LDD OC IND, Y STD	f Target.PWM > Average.PWM \ set output to true and store it in place \ of target.addr on stack				
		CLRA O2 IND, Y ADDD OA IND, Y STD	<ul> <li>\ add 255 to Average. PWM - Average. PWM/256</li> <li>\ and store it in place of the target page on</li> </ul>				
	ELS	E, FALSE IMM LDD OC IND, Y STD O2 IND, Y LDD OA IND, Y STD	<pre>\ the stack \ else just set output false \ and store Average. PWM - Average. PWM/256 \ in place of the target page on the stack</pre>				
	ENDIF, OG IMM LDAB ABY CALL !		<pre>\ in place of the target page on the stack \ drop top three stack cells \ we now have ( flag\new.avg\avg.xaddr ) \ store to Average.PWM</pre>				
	RTS BAS END						
\ This high level code is provided to help document the following assembly \ language version:							
$\langle \rangle \rangle \rangle \langle \rangle$	\`S \w \s	hich value to send to the bi ending PPA.Value to PPA all ocals{ &PPA.Value } \ bit place counter, ge	calling ?Update.PWM to determine t, and accumulating them in PPA.Value, then at once. ets doubled each iteration				
$\langle \rangle \rangle \langle \rangle \rangle$	n channel: * XN+ +PWM Value ?Update.PWM ed by ?Update.PWM send either a one or a zero: A. Value ENDIF A PIA. CHANGE. BITS						
	\ \$ \ w 01 DEY 00	date.PPA.Bits () \ Takes teps through the PPA bits, o hich value to send to the bi IMM LDAB OO IND,Y STAB IMM LDAB OO IND,Y STAB	calling ?Update. PWM to determine				
	IMM	.PWM Data +PWM Value SWAP LDD DEY DEY 00 IND, Y STD LDD DEY DEY 00 IND, Y STD	\ get xaddress of first PWM value \ put address on the stack \ put page on stack ( counter\ppa.value\xaddr )				

BEGIN,	( counter\ppa. value\xaddr )				
02 IND, Y LDD DEY DEY OO IND, Y STD	\ XDUP the xaddress				
02 IND, Y LDD					
DEY DEY OO IND, Y STD	$\land$ ( counter\ppa. value\xaddr\xaddr )				
CALL ?Update. PWM	( counter ppa. value xaddr fl ag )				
OO IND, Y LDD NE IF,	$\land$ test the flag				
O6 IND, Y LDAA	$\setminus$ add counter to ppa.value				
07 IND, Y ADDA	and counter to pper and				
06 IND, Y STAA					
ENDIF, 02 IMM LDAB ABY	$\land$ drop the flag ( counter $\pa.value\xaddr )$				
PPA. Record IMM LDD	\ get offset				
O2 IND, Y ADDD	$\setminus$ increment the address to point to the				
02 IND, Y STD	\ next desired PWM				
05 IND, Y ASL CS UNTIL,	\ increment the counter \ are we done?				
CS UNITL,	v are we done:				
04 IND, Y LDAB CLRA	$\setminus$ set up the stack for PIA. CHANGE. BITS				
04 IND, Y STD	\ put the value on the stack				
PPA. Bits. Used IMM LDD 00 IND, Y STD	<pre>\ get xaddress of PPA.Bits.Used \ put page on the stack</pre>				
IMM LDD 02 IND, Y STD	$\$ put addr on the stack ( ppa. value \xaddr )				
CALL C@	\ get PPA. Bits. Used ( ppa. value\ppa. bit. mask )				
PPA SWAP IMM LDD DEY DEY OO IND, Y STD	\ get xaddress of PPA \ put address on the stack				
IMM LDD DEY DEY OO IND, Y STD	\ put page on stack				
	$\$ stack now: (ppa. value\ppa. bit. mask\xaddr)				
CALL PIA. CHANGE. BITS RTS	\ send out the bits				
END. CODE					
: >PPA. PWM ( u\n )					
	value to send to PPA and $0 \le n \le 7$ is				
<pre>\ the PPA output bit number. Values of u from 0 to 256 are allowed, with 256 \ indicating a continuously ON condition. The time between updates of the</pre>					
\ output pins is determined by	the value of PERIOD, which holds the time				
$\land$ as the number of 2 usec tick	as of the TCNT clock.				
Locals{ & channel & value }					
&channel 0 MAX 7 MIN TO &chann &value 256 =					
IF					
1 & channel SCALE PPA. Bits.					
1 &channel SCALE PPA PIA. S ELSE	ET. BITS				
	cord &channel * XN+ +PWM Value C!				
\ The following two lines	are used if PWM update must be immediate				
\ rather than allowing over	er/undershoot for downstream averaging: ecord &channel * XN+ +PWM Value 1XN+ C!				
	ecord & channel * XN+ +PWM value IXN+ C! ecord & channel * XN+ +PWM Value 2XN+ C!				
\ we set PPA. Bits. Used aft	er setting the value so that we don't have				
\ transient update problem					
1 &channel SCALE PPA.Bits. ENDIF	USEU JEI. BIIJ				
;					

: >PERIOD ( n ) $\land$ n is the number of 2 microsecond clock ticks of TCNT between updates of $\land$ the PWMed D/A outputs. A period of 2 millisecond or 2000 microseconds $\land$ would require n = 1000 PERIOD ! ;	
: PWM Update.Interrupt.Service OC3.MASK TFLG1 C! \ Reset the OC3 interrupt flag so that new \ OC3 interrupts will be recognized. Because the flag is cleared by writin \ a one to it we can use a C! command without affecting the other bits. PERIOD @ TOC3 +! \ Add the PERIOD to TOC3 to set the time at which \ the next interrupt occurrs. Update.PPA.Bits \ Update the PPA output bits ;	ıg
<pre>: Install.PWM Update.Interrupt.Service OC3.MASK TMSK1 CLEAR.BITS \First we disable OC3 interrupts. OC3.MODE.MASK TCTL1 CLEAR.BITS \Set the OC3 mode and level bits so t OC3.LEVEL.MASK TCTL1 CLEAR.BITS \the timer is disconnected from output CFA.FOR PWM Update.Interrupt.Service \Attach the service routine. OC3.ID ATTACH OC3.MASK TFLG1 C! \Clear the OC3 interrupt flag. \We clear the OC3 interrupt flag by writing a one to it. This seems coun \intuitive but that's the way the hardware works! It makes sense when \we realize that we can just use a C! and not affect the other bits. \OC3.MASK TMSK1 SET.BITS \Finally, we enable OC3 interrupts. \Interrupts won't start until interrupts are also globally enabled by ENABLE.INTERRUPTS. Locally enabling the interrupts here is commented out \because, although it's a good idea for some applications, for this \application we don't want the interrupts starting until a separate \word, called Start.PPA.Update is executed. \.</pre>	t pin. ter-
; : Stop. PPA. PWM ( ) \Stops the PWMing outputs and sets them to zero. OC3. MASK TMSK1 CLEAR. BITS \Disables the OC3 interrupts. O PPA. Bits. Used C@ PPA PIA. CHANGE. BITS 8 0 DO O PPA. PWM Data PPA. Record I * XN+ +PWM Value C! O PPA. PWM Data PPA. Record I * XN+ +PWM Value 1XN+ ! LOOP ;	
: (Start.PPA.Update) Install.PWM Update.Interrupt.Service 1000 >PERIOD OC3.MASK TMSK1 SET.BITS \ Enables the OC3 interrupts ENABLE.INTERRUPTS \ and globally enables interrupts. ;	

Start. PPA. PWM ( -- ) Sets no bits for PWM output and initializes all bits for zero duty cycle. 0 PPA. Bits. Used C! 8 0 DO 0 PPA. PWM Data PPA. Record I \* XN+ +PWM Value **C**! 0 PPA. PWM Data PPA. Record I \* XN+ +PWM Value 1XN+ ! LOOP (Start. PPA. Update) : ReStart. PPA. PWM ( -- ) \ Restarts the PWM output updates but does not send them any duty cycles. \ That must be done with >PPA.PWM or >PPA.DAC (Start. PPA. Update)  $\land$  AXE out all words that the user doesn't need: AXE PERIOD AXE TOC3 AXE TCTL1 AXE TMSK1 AXE TFLG1 AXE OC3. MASK AXE OC3. LEVEL. MASK AXE OC3. MODE. MASK AXE PPA. Record AXE +PWM. Value AXE Info. for. PPA. PWM AXE PPA. PWM. Data AXE PPA. Bits. Used AXE ?Update. PWM AXE Update. PPA. Bits AXE Install. PWM Update. Interrupt. Service AXE PWM Update. Interrupt. Service AXE (Start. PPA. Update) \*\*\*\*\*\* ١ \* \* \*\*\*\*\*\* End of Code ١

This application note is intended to assist developers in using the QED Board. The information provided is believed to be reliable; however, Mosaic Industries assumes no responsibility for its use or misuse, and its use shall be entirely at the user's own risk. Any computer code included in this application note is provided to customers of the QED Board for use only on the QED Board. The provision of this code is governed by the applicable QED software license. For further information about this application note contact: Paul Clifford at Mosaic Industries, Inc., (510) 790-1255.

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