

Greater Resolution for the QED's 8-bit DAC

Summary

The following describes how to get greater resolution for the QED's 8-bit DAC.

Description

Often greater resolution is needed than that provided by the QED Board's 8-bit DAC. One solution is to combine two DAC channels in hardware to produce a single channel of greater resolution. This solution is implemented by the QED Analog Conditioning Board, on which two pairs of channels are combined with their output calibrated against the 12-bit A/D, or any other pairs combined without direct calibration. This application note provides another solution: The output of any of the DAC channels can be modulated so that it rapidly flickers between two adjacent levels. After the output is averaged with a low pass filter, up to 256 discrete analog voltages can be produced within each step of the 8-bit DAC. Resolutions up to 16 bits can be produced (given sufficient averaging time), but without the true accuracy of 16-bit D/A converter. The absolute accuracy is still limited to that of the 8-bit DAC itself. Even so, this accuracy is generally better than 8bits; it is approximately 10-11 bits without calibration, and if calibrated against the 12-bit A/D, better than 12bits resolution with 12-bits of accuracy can be attained.

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Ň	*****	This code is provided to customers of the QED Board	* * * * * * * * *
Ň	****	for use with the QED Board Software Development	* * * * * * * * *
Ň	*****	environment. The provision of this code is governed	* * * * * * * * *
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///////////////////////////////////////	This program writes 16-bivalues between the standar between two adjacent leve each step of the 8-bit DA of the DAC a low pass fil- value with a small residural algorithm that is optimal time to achieve a given leve	t values to the 8-bit DAC cha rd 8-bit levels are achieved ls (i.e., pulse width modulat C is divided into 256 smaller ter smooths the flickering le al ripple. The flickering is in the respect that it requi evel of resolution.	annels. Intermediate by rapidly flickering ting). In this way r steps. Downstream evels into an average s done using a PWM res the least averaging
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$\langle \rangle$	****	ndan tha Uaad. Naw It Wanka	*****
``	**********U	nder the Hood: How It Works	* * * * * * * * *
$\langle \rangle$	****	* * * * * * * * * * * * * * * * * * * *	*****
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$\langle \rangle$	For a detailed descriptio Application Note "MI-AP-O	n of the PWM algorithm see th 56: A PWM Algorithm with Opti	ne Mosaic Industries QED mal Averaging Properties".
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	An interrupt service rout be adjusted from a minimu the DAC channels) to as m constant of t seconds or DACs time to settle to a downstream filtering time For example, with an inte filter time constant of 8 minimum, and the DAC reso of 16) to 12-bits. This value of 5 msec; I recomm 0.1 second be used.	ine services the DACs every t m of about 3 msec (it takes 2 uch as 131 msec. Downstream less would result in signific resolution of only 8-bits. H adds an additional bit of re rrupt service time set to 5 m 0 msec or greater the filter lution would be increased by code sets the interrupt servi end that a downstream filteri	2. Seconds, where t can 2. 36 msec to service all filtering with a time cant ripple, allowing the Each doubling of the esolution to the DAC. msec and a downstream time is 16 times the 4 bits (the base 2 log ce time to a default ng time constant of
///////////////////////////////////////	Although this program suc smaller steps, the DAC st linearity than it started and to have an integral n temperature range of -40° (for the Analog Devices D over the entire temperatu step accuracy is really a The algorithm of this pro- take advantage of that ac	cessfully divides each 8-bit ill does not have any better with. It is guaranteed to b onlinearity of typically +/-1 C to +85°C. However, if we e AC-8841F) we find that its pe re range is typically +/- 1/8 pproximately 10 to 11 bits, r gram allows us to increase it curacy.	DAC step into 256 absolute accuracy or be monotonic to 8-bits, 1/2 lsb, over an ambient examine its Data Sheet er step linearity error 8 lsb. So its step to cather than just 8-bits. cs resolution to better
$\langle \rangle$ $\langle \rangle$ $\langle \rangle$	In tests of the program of is a maximum error of 1.5 is, the maximum fractiona 11 bits of accuracy.	ver the entire range of D/A o millivolts for a 3.0 volt fu l error is one part in two th	output I find that there all scale output. That nousand, or there is

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* * * *	* * * * *	How to Use It	* * * * * * * * * *
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To us	e this higher 1	resolution option perform the follow	ing steps:
1.	Connect the QI 100 microfarao corresponding resolution.	ED Board to an Analog Conditioning Bo l capacitors in board at locations FI to the DAC channels you wish to use This provides a 0.1 second output fil	oard and insert D1, FD2FD8 for greater lter time constant.
2.	Insert gain re GD1, GD2GD8 to scale the r still sourcing current capabi nominally 13.	esistors on the Analog Conditioning H corresponding to the DAC channels y maximum DAC output to voltages as gre y up to 10 ma, and about 11.5 volts y lity. (The maximum voltage is the s +/13 volts less the op-amp headro	Board at locations you wish to use eat as 10.2 volts while with little source supply voltage of oom of 1.5 volts.)
3.	If you wish to higher resolut rapid than 5 m use this softw as the high on order byte to the desired 8- that channel. If you need up while at the s will need to m	continue using some channels as 8-b tion DACs, and you do not require upon msec then you can continue to use this vare, but pass the desired 8-bit value of the byte of its 16-bit integer input zero. This program will then update bit value within 5 msec, and there we You do not need a low pass filter of odates on an 8-bit channel more rapic same time requiring high resolution of modify this code appropriately.	bit DACs rather than date times more is code. You can just ue to >Hi.Res.DAC t and set the low e the DAC channel with will be no flicker on on that channel. d than every 5 msec channels then you
4.	Download this	text file.	
5.	Execute Start. DAC service in 5 msec.	DAC to initialize all DAC outputs to iterrupt, and start up the periodic I	to zero, attach the DAC update every
6.	Send 16-bit in >Hi. Res. DAC wh takes as input The DAC output value one grea (LSB), so that is produced co The minimum ou with all codes FFFF all resul inputs/outputs output, Vmax, be u = 65280 *	itegers to the desired DAC channel us ich has the stack picture ( $u n - $ ); a 16-bit unsigned value, u, and the flickers between the most significa- iter, MSB+1, with a duty cycle detern after adequate low-pass filtering a presponding to one of 256 levels in itput code is 0000 hex, and the maxin in between represented. Note that t in the maximum output. There are s. To produce an output voltage, V, the unsigned value that must be sent V / Vmax.	sing the word ). This top level word e DAC channel number, n. ant byte (MSB) and the mined by the lower byte an average analog voltage between MSB and MSB+1. mum output code is FF00, codes between FF00 and 255*256 = 65280 possible given a full scale t to >Hi. Res. DAC would

To calibrate a DAC channel send FF00 to the channel using >Hi.Res.DAC and measure the voltage produced. This voltage is then used to determine the code sent to a DAC channel to produce any voltage. For example, 7. ١ \ suppose the voltage measured for channel #3 is 10.31 volts. \ The following code sends any desired voltage up to 10.31 volts to DAC channel 3: 10.31 FCONSTANT Vmax#3 \ a constant to hold the maximum output \ voltage : > Channel #3 (r --) $\ r$  is a floating point number representing the voltage to  $\ send$  to channel #3 Vmax#3 F/ 0.0 FMAX \ limit the input voltages to positive values 1.0 FMIN  $\setminus$  limit the input to less than the maximum 65280. F* UFIXX 3 >Hi. Res. Dac You would then send a voltage, for example 5.2 volts to that DAC channel by executing: 5. 2 > Channel #3 8. To stop updating the DACs execute Stop. DAC and the interrupt service routine will stop. The DACs will be left set to the 8-bit level either just greater or less than the 16-bit value sent to them. Because this routine uses the kernel word (>DAC) which does not expect SPI resource conflicts, it does not call SPI.RESOURCE GET and RELEASE. Consequently, this routine should not be used when other hardware (for example the 12-bit A/D) may also require the SPI. 9. If you want to use routine in conjunction with other code that also uses the SPI then you should disable interrupts around the other user of the SPI. For example, to use the 12-bit A/D, instead of calling the word A/D12. SAMPLE you would execute the sequence: DI SABLE. I NTERRUPTS (A/D12. SAMPLE) ENABLE. I NTERRUPTS in which the faster flavor of the A/D word is used ( (A/D12.SAMPLE) instead of A/D12.SAMPLE ) which doesn't call GET or RELEASE because that's not necessary if interrupts are disabled around all SPI using words. For example if you want to measure a signal from a temperature transducer on the A/D12 channel #4 you could write a word like the following: : Get. Temperature ( -- u ) \ u is an unsigned integer representing the temperature \ put a flag on the stack for single ended, - 1 \ unipolar conversion 4 \ the A/D channel number between 0 ad 7 DISABLE. INTERRUPTS (A/D12. SAMPLE) ENABLE. INTERRUPTS

$\$ The following are descriptions of all the user words:
<pre>\ Start.DAC ( )     \ Initializes DAC outputs to zero and starts up their periodic interrupt     \ service.</pre>
<pre>\ Stop. DAC ( )</pre>
<pre>\ ReStart.DAC ( )</pre>
$\label{eq:hi.Res.DAC} (u \ n \ ) \\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$
<pre>&gt;PERIOD (u)     \ u is and unsigned integer representing the number of 2 microsecond clock     \ ticks of TCNT between updates of the PWMed D/A outputs. A period of 5     \ milliseconds would require u = 2500. PERIODs less than 5 msec are not     \ recommended as the servicing of all 8 DAC channels takes about 2.5 msec.     \ If the PERIOD is too small interrupts will be missed and full TCNT     \ rollover periods of 131 msec will be inserted as delays into the interrupt     \ servicing. The PERIOD is initialized to 5 msec by Start. DACs, and can     \ be changed thereafter by &gt;PERIOD.     *********************************</pre>
\ ********       *********         \ ********       Warnings!         *********
\ ************************************
Note: The following routine uses the kernel word (>DAC) which does not expect SPI resource conflicts so does not call SPI. RESOURCE GET and RELEASE. Consequently, this routine should not be used when other hardware (for example the 12-bit A/D) may also require the SPI. If you want to use this in an multitasking environment, or in conjunction with other code that also uses the SPI then you would generally need to replace the call to (>DAC) in the word Update. DAC. Values with a call to >DAC instead. However, in this case, that solution is unsufficient. Because the call occurrs from within an interrupt service routine, the GET would loop forever if the SPI is not free because the interrupts that switch tasks are disabled while the interrupt service routine runs (interrupts are not allowed to nest). A solution is to continue to use (>DAC) but to disable interrupts around any other uses of the SPI in any tasks so that this interrupt service routine never attempts to use the SPI while it is otherwise in use. Because (>DAC) is called by this code from within an interrupt service routine other users of the SPI will not be able to interrupt (>DAC)'s use of it so that is not a concern.

\ The Code \ ****** \ ANEW <Hi. Res. DACs>  $\setminus$  Holds the period between interrups as the number of  $\setminus$  2 microsecond ticks of TCNT. A value of 2500 VARIABLE PERIOD  $\land$  corresponds to 5 msec. HEX 801A REGISTER: TOC3 8020 REGISTER: TCTL1 8022 REGISTER: TMSK1 8023 REGISTER: TFLG1 CONSTANT OC3. MASK CONSTANT OC3. LEVEL. MASK CONSTANT OC3. MODE. MASK 20 10 20 DECI MAL Structure. Begin: DAC. Channel. Record TYPE. OF: I NT - >+DAC. Value \ for the 16-bit unsigned value to be written **1 RESERVED**  $\setminus$  for the low order byte of the Target.PWM OR. TYPE. OF: **1 RESERVED**  $\setminus$  for the MSB to be sent directly to the DAC  $\$  for the lower order byte of the DAC value  $\$  (the high byte of Target. PWM) to be PWMed I NT- > +Target. PWM TYPE. END  $\land$  for use as Average. PWM by ?Update. DAC. PWM 2 RESERVED BYTE - >+Greater. DAC. Value  $\setminus$  for the MSB+1 to be sent to the DAC Structure. End \ Create a single structure containing all eight DAC channel records: Structure. Begin: All. DAC. Info 8 DAC. Channel. Record STRUCTS-> +DAC. Info. Start Structure. End \ Now we instantiate (reserve space for) the DAC. Info structure in variable  $\land$  space: All. DAC. Info V. INSTANCE: DAC. Info

 $\$  If we were not to use the above DAC data structure we would need the following  $\$  two variables for each DAC channel. They are shown here only for clarity. \ The variable Average. PWM must directly follow the variable Target. PWM  $\land$  in memory.  $\land$  VARIABLE Target.PWM  $\land$  Holds the target PWM as an 8-bit number in the high order \ byte. The contents of the low order byte are irrelevant. Fetch or store to  $\setminus$  this variable using C@ and C!. VARIABLE Average. PWM \ Used internally by the algorithm; holds a running \ average PWM To update the PWM immediately set both Target. PWM and Average. PWM \ to the new value. To update the 256-bit long integral of the output most \ quickly do not modify Average. PWM when Target. PWM is reset. The Average. PWM \ is set by setting its high order byte to the desired PWM (0-255) and setting \ is to have and a base to 255  $\setminus$  its low order byte to 255.  $\setminus$  The following is a high level version of the corresponding assembly language \ routine. It is provided here for documentary purposes only: ?Update. DAC. PWM ( xaddr -- Flag )  $\$  This word implements as PWM routine that optimally averages.  $\$  xaddr is the address of Target. PWM and xaddr+2 is the address of  $\mathbf{1}$  $\mathbf{1}$  $\land$  Average. PWM, both as 16-bit unsigned integers. \ \ Flag is the bit to be outputted, either true for high or false for low. \ Each time Update. PWM is called Flag is set to either true or false \ \ \  $\setminus$  to maintain the proper average value for the PWM output. \ [ BASE @ HEX ] XDUP 2 XN+ . \ \ Locals{ x&Average.addr x&Target.addr } \ \ \ x&Target. addr @ FF00 AND x&Average. addr @ U> IF x&Average. addr @ x&Average. addr C@ - 00FF + x&Average. addr ! 111 TRUE ELSE x&Average. addr @ x&Average. addr C@ x&Average. addr ! / FALSE ENDI F \ [ BASE ! ] \ \ The following code is an assembly language version of the above high level  $\land$  routine. CODE ?Update.DAC.PWM ( xaddr -- Flag )  $\$  xaddr is the address of Target.PWM and xaddr+2 is the address of  $\$  Average. PWM, both as 16-bit unsigned integers.  $\$  Flag is the bit to be outputted.  $\$  Each time Update.PWM is called Flag is set to either true or false  $\land$  to maintain the proper average value for the PWM output. BASE @ HEX 02 IND, Y LDD \ Get the Target. PWM address 02 IMM ADDD  $\setminus$  and increment by 2 and push it on the stack  $\land$  as the Average. PWM address. DEY DEY OO IND, Y STD 02 IND, Y LDD \ Fetch, DEY DEY OO IND, Y STD  $\setminus$  and push the page too. \ Then XDUP the Average. PWM xaddress 02 IND, Y LDD DEY DEY OO IND, Y STD

02 IND, Y LDD DEY DEY OO IND, Y STD  $\land$  @ Average. PWM and push it CALL @ \ get Average. PWM/256 OO IND, Y LDAB CLRA DEY DEY OO IND, Y STD push Average. PWM/256 02 IND, Y LDD 00 IND, Y SUBD 00 IND, Y STD \ replace Average. PWM/256 on tos with \ Average. PWM - Average. PWM/256 \ put Target address on tos
\ put Target page on tos OA IND, Y LDD DEY DEY OO IND, Y STD OA IND, Y LDD DEY DEY OO IND, Y STD @ Target. PWM and push it CALL @ \ get target from stack 00 IND, Y LDD CLRB zero out the low order byte 04 IND, Y CPD ∖ Target. PWM - Average. PWḾ \ if Target. PWM > Average. PWM HI IF. TRUE IMM LDD OC IND. Y STD  $\setminus$  set output to true and store it in place  $\land$  of target. addr on stack  $\backslash$  add 255 to Average. PWM - Average. PWM/256  $\backslash$  and store it in place of the target page on CLRA 02 IND, Y ADDD OA IND, Y STD \ the stack ELSE. FALSE IMM LDD OC IND, Y STD  $\land$  else just set output false 02 IND, Y LDD OA IND, Y STD \ and store Average. PWM - Average. PWM/256 \ in place of the target page on the stack ENDIF. **06 IMM LDAB ABY** \ drop top three stack cells  $\land$  we now have ( flagnew. avg avg. xaddr ) CALL !  $\land$  store to Average. PWM RTS BASE ! END. CODE \ This high level code is provided to help document the following assembly  $\land$  language version: Update. DAC. Values  $\setminus$  takes 2.36 msec  $\$  Steps through the DAC channels, calling ?Update. DAC. PWM to determine  $\$  which value to send to the DAC, and sends it. \ ١ \ 8 0 / / / / / DO \ Call ?Update. DAC. PWM for a channel: DAC. Info DAC. Channel. Record I * XN+ XDUP +Target. PWM ?Update. DAC. PWM ackslash Depending on flag returned by ?Update.DAC.PWM send either the DAC's \ eight bit value or a value one greater: IF +Greater. DAC. Value ELSE +DAC. Value ENDIF \ C@ I 1+ (>DAC) LOOP \ ;

CODE Update.DAC.Values ( -- )  $\setminus$  This version takes 1.6 milliseconds. \ Steps through the DAC channels, calling ?Update. DAC. PWM to determine  $\setminus$  which value to send to the DAC, and sends it. CLRA 01 IMM LDAB DEY DEY 00 IND, Y STD DAC. Info +Target. PWM SWAP \ load counter value into B  $\$  and put counter on stack ( counter )  $\$  get xaddress of first target.pwm IMM LDD DEY DEY OO IND, Y STD  $\setminus$  put address on the stack IMM LDD DEY DEY OO IND, Y STD  $\ \$  put page on the stack ( counter $\xaddr$  ) BEGIN. ( counter\xaddr ) 02 IND, Y LDD  $\land$  XDUP the xaddress DEY DEY OO IND, Y STD 02 IND, Y LDD DEY DEY OO IND, Y STD O2 IND, Y LDD DEY DEY OO IND, Y STD  $\setminus$  XDUP the xaddress 02 IND, Y LDD DEY DEY OO IND, Y STD \ ( counter\xaddr\xaddr\xaddr ) CALL ?Update. DAC. PWM \ ( counter\xaddr\xaddr\flag ) 00 IND, Y LDD  $\land$  test the flag EQ IF, 04 IND, Y LDD  $\land$  modify address to point to +DAC. Value 01 IMM SUBD 04 IND, Y STD ELSE, 04 IND, Y LDD  $\land$  modify address to point to +Greater. DAC. Value 04 IMM ADDD 04 IND, Y STD ENDIF. 02 IMM LDAB ABY  $\land$  drop the flag  $\land$  ( counter $\xaddr\value$  ) CALL C@ 06 IND, Y LDD \ get the channel#, the counter DEY DEY OO IND, Y STD  $\land$  and push it and call (>DAC) CALL (>DAC) \ ( counter\xaddr ) 02 IND, Y LDD \ increment the target address \ to point to next DAC channel record 06 IMM ADDD 02 IND, Y STD 05 IND, Y INC \ increment the counter 09 IMM LDAA \ load terminal count into A 05 IND, Y CMPA  $\setminus$  and compare it to the counter EQ UNTIL,  $\setminus$  to see if we're done 06 IMM LDAB ABY  $\land$  drop the stack RTS **END. CODE** 

: >Hi. Res. DAC ( $u \setminus n - -$ )  $\setminus$  u is an unsigned 16-bit value to send to the DAC and 1 <= n <= 8 is  $\$  the channel number. The minimum value for u is 0000 hex, and  $\$  the maximum is FF00, with all codes in between represented. Note  $\$  that codes between FF00 and FFFF all result in the maximum output.  $\land$  There are 255*256 = 65280 possible inputs/outputs. To produce an output  $\$  voltage, V, given a full scale output, Vmax, the unsigned value that must  $\$  be sent to >Hi. Res. DAC would be u = 65280 * V / Vmax. 1-  $\$  convert channel number to 0...7 range Locals{ & channel & value } \ First store zero to the Target. PWM and Average. PWM 0\0 DAC. Info DAC. Channel. Record & channel * XN+ + Target. PWM 2! \ Store the full 16-bit value in the DAC. Info data structure  $\setminus$  This puts the MSB in the +DAC. Value location and the LSB in \ the +Target. PWM location &value DAC. Info DAC. Channel. Record & channel * XN+ +DAC. Value ! \ Store the lower byte in the Average. PWM &value DAC. Info DAC. Channel. Record & channel * XN+ + Target. PWM 2XN+ C! ∖ Store the MSB+1 to the +Greater. DAC. Value &value -8 SCALE \ shift value over 8 places to get high order byte 255 AND  $\land$  blank out new top byte MIN 1+ \ increment by one but don't allow rollover from 255 to 256 DAC. Info DAC. Channel. Record & channel * XN+ +Greater. DAC. Value C! 254 MIN 1+ : > PERIOD (n - -) $\setminus$  n is the number of 2 microsecond clock ticks of TCNT between updates of \ the PWMed D/A outputs. A period of 1/2 millisecond or 500 microseconds  $\setminus$  would require n = 250 PERIOD ! : D/A. Update. Interrupt. Service OC3 interrupts will be recognized. Because the flag is cleared by writing  $\$  a one to it we can use a C! command without affecting the other bits. PERIOD @ TOC3 +! \ Add the PERIOD to TOC3 to set the time at which \ the next interrupt occurrs. Update.DAC.Values \ Update the 8 DAC channels

: Install. D/A. Update. Interrupt. Service \ First we disable OC3 interrupts. OC3. MASK TMŠK1 CLEAR. BITŠ \ Set the OC3 mode and level bits so that OC3. MODE. MASK TCTL1 CLEAR. BITS OC3. LEVEL. MASK TCTL1 CLEAR. BITS  $\setminus$  the timer is disconnected from output pin. CFA. FOR D/A. Update. Interrupt. Service  $\setminus$  Attach the service routine. OC3. ID ATTACH OC3. MASK TFLG1 C! \ Clear the OC3 interrupt flag. \ We clear the OC3 interrupt flag by writing a one to it. This seems counter- $\setminus$  intuitive but that's the way the hardware works! It makes sense when  $\setminus$  we realize that we can just use a C! and not affect the other bits. \ OC3. MASK TMSK1 SET. BITS \ Finally, we enable OC3 interrupts. \ Interrupts won't start until interrupts are also globally enabled by \ ENABLE. INTERRUPTS. Locally enabling the interrupts here is commented out \ because, although it's a good idea for some applications, for this
\ application we don't want the interrupts starting until a separate
\ word, called Start.Periodic.D/A.Update, is executed. : Stop. DAC ( -- ) 0C3. MASK TMSK1 CLEAR. BITS  $\land$  Disables the 0C3 interrupts. Start. Peri odi c. D/A. Update Install. D/A. Update. Interrupt. Service 2500 > PERIODOC3. MASK TMSK1 SET. BITS **\ Enables the OC3 interrupts** ENABLE. INTERRUPTS  $\land$  and globally enables interrupts. : Start. DAC ( -- ) 9 1 DO 0 I >Hi. Res. DAC LOOP Init. A/D12&DAC Start. Periodic. D/A. Update : ReStart. DAC ( -- ) Start. Peri odi c. D/A. Update  $\setminus$  AXE out all words that the user doesn't need: AXE DAC. Channel. Record AXE +DAC. Value AXE +Target. PWM AXE All. DAC. Info AXE +DAC. Info. Start AXE +Greater. DAC. Value AXE ?Update. DAC. PWM AXE Update. DAC. Values AXE DAC. Info AXE PERIOD AXE D/A. Update. Interrupt. Service AXE TCTL1 AXE TOC3 AXE TFLG1 AXE TMSK1 AXE OC3. LEVEL. MASK AXE OC3. MODE. MASK AXE OC3. MASK AXE Install. D/A. Update. Interrupt. Service AXE Start. Periodic. D/A. Update ******* \ ******* / End of Code ١ \ ١

This application note is intended to assist developers in using the QED Board. The information provided is believed to be reliable; however, Mosaic Industries assumes no responsibility for its use or misuse, and its use shall be entirely at the user's own risk. Any computer code included in this application note is provided to customers of the QED Board for use only on the QED Board. The provision of this code is governed by the applicable QED software license. For further information about this application note contact: Paul Clifford at Mosaic Industries, Inc., (510) 790-1255.

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