



Summary

The following explains how to set up input capture 1 to interrupt when a debounced rising edge occurs.

edge occurs on IC1, which is port A, pin 2. This software also debounces the input capture, if an unbounced mechanical switch is used to trigger the interrupt, only one interrupt will occur. It is up to the user to determine the needed debounce time either via inspection of switch data sheets or via testing.

Description

This app-note shows how to use the input capture hardware to generate an interrupt whenever a rising

The debouncing works by using the timeslicer, which uses output compare 2 (OC2). The timeslicer does not affect any hardware pins.

HEX

8 WIDTH !

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8022 REGISTER: TMSK1      \ timer interrupt mask register #1
8023 REGISTER: TFLG1     \ timer interrupt flag register #1
8021 REGISTER: TCTL2     \ timer control reg. #2, holds edge specification bits
4    CONSTANT  IC1.MASK  \ mask to set and clear IC1F and IC1I
10   CONSTANT  EDG1A.MASK \ mask to set edge
20   CONSTANT  EDG1B.MASK \ mask to set edge

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DECIMAL

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DIN 20 2CONSTANT DEBOUNCE.TIME      \ 20 * 5ms = 100 ms debounce time
                                           \ adjust this for your application

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2VARIABLE LAST.TIME                \ To keep track of debounce time

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: IC1.ISR (--)

\ Interrupt Service Routine for IC1

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    IC1.MASK TFLG1 C!                \ Clear interrupt flag
    TIMESLICE.COUNT 2@ 2DUP LAST.TIME 2@ D- \ Calculate time from last
                                           \ successful interrupt

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    DEBOUNCE.TIME D>                \ If we've waited long enough
    IF

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\ add your code here

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    ELSE LAST.TIME 2!                \ Update time

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    2DROP                            \ Drop time

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ENDIF

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: IC1. INTERRUPT. DISABLE ( -- )
  IC1. MASK TMSK1 CLEAR. BITS      \ disable IC1 interrupts
  STOP. TIMESLICER                 \ Stop timeslicer interrupts
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: IC1. INTERRUPT. INIT ( -- )
  IC1. MASK PORTA. DIRECTION CLEAR. BITS \ setup port A direction (DDRA)
                                          \ pin 2 as input
  IC1. MASK TMSK1 CLEAR. BITS          \ disable IC1 interrupts while we are
                                          \ setting up
  \ Here we configure the TCTL2 to set the interrupt to trigger on a
  \ rising edge only
  EDG1A. MASK TCTL2 SET. BITS           \ Set EDG1A to 1
  EDG1B. MASK TCTL2 CLEAR. BITS         \ Set EDG1B to 0
  CFA. FOR IC1. ISR IC1. ID ATTACH      \ install handlers
  IC1. MASK TFLG1 C!                    \ Clear interrupt flag
  IC1. MASK TMSK1 SET. BITS              \ set IC1I mask bit
  INIT. ELAPSED. TIME                   \ Zeros the timeslicer
  TIMESLICE. COUNT 2@ LAST. TIME 2!     \ Initialize CURRENT. TIME variable
  START. TIMESLICER                     \ Starts timeslicer and globally
                                          \ enables interrupts
;

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