

Setting Up Input Capture 1 to Interrupt on Rising Edge

APPLICATION NOTE MI-AN-041

Summary

This app-note shows how to use the input capture hardware to generate an interrupt whenever a rising edge occurs on IC1, which is port A, pin 2. This software does not debounce the input capture, if an unbounced mechanical switch is used to trigger the interrupt, several interrupts may occur.

```
8 WIDTH!
HEX
8022
       REGI STER:
                    TMSK 1
                                   \ timer interrupt mask register #1
                                   \ timer interrupt flag register #1 \ timer control reg. #2, holds edge specification bits
8023
       REGI STER:
                    TFLG1
8021
       REGI STER:
                    TCTL2
                                   \ mask to set and clear IC1F and IC1I
                    IC1. MASK
       CONSTANT
10
       CONSTANT
                    EDG1A. MASK
                                   \ mask to set edge
       CONSTANT
                    EDG1B. MASK
                                   \ mask to set edge
 IC1. ISR ( -- )
\ Interrupt Service Routine for IC1
       IC1. MASK TFLG1 C!
                                                 \ Clear interrupt flag
       \ add your code here
  IC1. INTERRUPT. DI SABLE ( -- )
       IC1. MASK TMSK1 CLEAR. BITS
                                                 \ disable IC1 interrupts
 IC1. INTERRUPT. INIT ( -- )
       IC1. MASK PORTA. DIRECTION CLEAR. BITS \ setup port A direction (DDRA) pin 2
                                                      as input
       IC1. MASK TMSK1 CLEAR. BITS
                                                   disable IC1 interrupts while we are
                                                      setting up
       \setminus Here we configure the TCTL2 to set the interrupt to trigger on a
       rising edge only
EDG1A. MASK TCTL2 SET. BITS
EDG1B. MASK TCTL2 CLEAR. BITS
                                                 \setminus Set EDG1A to 1
                                                  \setminus Set EDG1B to 0
       CFA. FOR IC1. ISR IC1. ID ATTACH
                                                 \ install handlers
                                                 \ Clear interrupt flag
\ set IC1I mask bit
       IC1. MASK TFLG1 C!
       IC1. MASK TMSK1 SET. BITS
       ENABLE. INTERRUPTS
                                                 \ Globally enable interrupts
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