Summary

This code demonstrates a simple method to set up the COP (watchdog timer) in a production version of the QED Board.

Description

THREE CONSECUTIVE HARDWARE RESETS are required to install and secure the COP after the production PROM is first installed into the board.

Note: you can simultaneously "lock down" (make unwritable) some or all of the contents of EEPROM by hanging the value written to BPROT during the UNLOCK.CONFIG operation.

Note: it's best to leave the COP response vector initialized to point to the standard reset routine as it is by default; see INIT.VITAL.IRQS.ON.COLD. Otherwise the HC11's 64cycle timingrestrictions for special registers may not be met.

COP definitely performs a hardware init of all processor registers. 11/93.


```
HEX
4 USE.PAGE
8 WIDTH !
ANEW COP.TEST.CODE

8024 REGISTER: TMSK2
8025 REGISTER: TFLG2
8026 REGISTER: PACTL
802B REGISTER: BAUD
8035 REGISTER: BPROT
8039 REGISTER: OPTION
803A REGISTER: COPRST
803F REGISTER: CONFIG
 4  CONSTANT COP.DISABLE.MASK      \ in CONFIG; COP is off if bit is set
10  CONSTANT LOCK.CONFIG.MASK      \ in BPROT; prevents writes to CONFIG
03  CONSTANT COP.TIMEOUT.MASK      \ lowest 2 bits in OPTION control timeout
03  CONSTANT COP.TIMEOUT.PERIOD    \ pick desired period;see pg. 6-3 in F1 book
3   CONSTANT RTI.RATE.MASK         \ set lower 2 bits in PACTL to 11 for 32.77ms rate
40  CONSTANT RTI.MASK              \ local irq mask in TMSK2; flag mask in TFLG2

: RTI/COP.SERVICE    ( -- )
    >ASSM                         \ first service the COP
        55AA IMM LDD
        COPRST DROP EXT STAA
        COPRST DROP EXT STAB
    >FORTH
    RTI.MASK TFLG2 C!             \ clear the irq flag bit
    ;
```

```
      : ENABLE.REAL.TIME.INTERRUPT    ( -- )
    \ installs service routine and enables local irq mask
    \ and sets rate to 32.77 msec;
    \ does NOT globally enable interrupts
    CFA.FOR RTI/COP.SERVICE RTI.ID ATTACH
    RTI.RATE.MASK PACTL  SET.BITS          \ set rate
    RTI.MASK TMSK2 SET.BITS                \ locally enable interrupt
    ;
: COP.DISABLED?    ( -- flag )     \ true if cop is disabled
    CONFIG C@ COP.DISABLE.MASK AND BOOLEAN
    ;

: CONFIG.LOCKED?    ( -- flag )    \ true if we can't write to config
    BPROT C@ LOCK.CONFIG.MASK AND BOOLEAN
    ;

: UNLOCK.CONFIG    ( -- )
    OPTION C@
    COP.TIMEOUT.MASK COMPLEMENT AND COP.TIMEOUT.PERIOD OR     \ set COP timeout
    TMSK2 C@                                  \ TMSK2 is unchanged
    BPROT C@ LOCK.CONFIG.MASK COMPLEMENT AND  \ allow writes to config reg
    BAUD C@                                   \ BAUD is unchanged
    INSTALL.REGISTER.INITS                    \ takes effect after next hardware
reset
    ;

: ENABLE.COP    ( -- )
    \ assumes that CONFIG register is writable now;
    \ writes to CONFIG's EEPROM backup cell to enable COP, effective upon
    \ the next hardware reset.
    \ Also installs register inits that set COP timeout period
    \ and protect config register.  These also take effect upon next reset.
    CONFIG C@ COP.DISABLE.MASK COMPLEMENT AND
    CONFIG DROP (EEC!)                \ enable COP by clearing bit 2 in config
    OPTION C@
    COP.TIMEOUT.MASK COMPLEMENT AND COP.TIMEOUT.PERIOD OR    \ set COP timeout
    TMSK2 C@                                                 \ TMSK2 is unchanged
    BPROT C@ LOCK.CONFIG.MASK OR                             \ protect config reg
    BAUD C@                                                  \ BAUD is unchanged
    INSTALL.REGISTER.INITS
    ;
: INSTALL.COP    ( -- )
    COP.DISABLED?
    IF CONFIG.LOCKED?
        IF      UNLOCK.CONFIG     \ takes effect upon next hardware reset
        ELSE    ENABLE.COP        \ takes effect upon next hardware reset
        THEN
    THEN
    ;
```

```
: TOP.WORD    ( -- )
    RTI/COP.SERVICE
    ENABLE.REAL.TIME.INTERRUPT        \ this is the COP service routine
    INSTALL.COP                       \ may take full effect upon the 3rd reset
    ENABLE.INTERRUPTS                 \ enable RTI; comment out to force failure
    ;

CFA.FOR TOP.WORD AUTOSTART
 SAVE
```


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