# Signal Conditioning Wildcard User Guide

Version 1.0
November, 2006

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*The Signal Conditioning Wildcard is used with the Analog I/O Wildcard to increase its input and output voltage range and to add 4-20 mA current input and output capability This document describes the capabilities of the Signal Conditioning Wildcard and tells how to connect and use it with an Analog I/O Wildcard.*

## Specifications

| 0–10 V Voltage Inputs | |
|---|---|
| Input Channels | 4 unipolar single-ended; pairs of channels may be used for differential input |
| Resolution | 16-bits ( 0 – 65,535 counts) |
| Input Voltage Range | 0 to 10.24 V is converted to 0-2.048 V presented to the Analog I/O Wildcard (range customizable by component substitution) |
| Input Filtering | Single-pole 265 Hz low-pass filter, reconfigurable by component substitution |
| Input Impedance | 376 KΩ |
| Offset and Scale Errors | ±0.1% of FS offset error and ±1-2% of FS gain error are added to any A/D offset and gain errors |

| 0–10 V Voltage Outputs | |
|---|---|
| Output Channels | 4 unipolar single-ended |
| Resolution | 12-bits ( 0 – 4095 counts) |
| Full Scale Output Voltage | 0 to 10.24 V is produced from 0-4.096 V provided by the Analog I/O Wildcard (range customizable by component substitution) |
| Settling Time | 300 μsec typically, slew rate is 0.1V/μsec |
| Allowed Load Resistance | ≥ 1KΩ, Op-amp output sources and sinks up to 10 mA, sink current limited at $V_o$=0 by 39Ω output resistance. |
| Offset and Scale Errors | ±0.05% of FS offset error and ±1-2% of FS gain error are added to any A/D offset and gain errors |

| 0–20 mA Current Inputs | |
|---|---|
| Input Channels | 4 unipolar single-ended current sinks |
| Resolution | 16-bits ( 0 – 65,535 counts) |
| Input Current Range | 0 to 20.48 mA is converted to 0–2.048 V presented to the Analog I/O Wildcard (range customizable by component substitution) |
| Input Protection | Protected to -30V, +15V, or +100 mA steady state input |
| Input Resistance | 200 Ω (for up to 50 mA input, dynamic resistance drops toward 100 Ω for greater currents) |
| Offset and Scale Errors | No offset error and ±1% of FS gain error is added to any A/D offset and gain errors |

| 0–20 mA Current Outputs | |
|---|---|
| Output Channels | 4 unipolar single-ended current sources |
| Resolution | 12-bits ( 0 – 4095 counts) |
| Output Current Range | 0 to 20.48 mA is produced from 0–4.096 V provided by the Analog I/O Wildcard (range customizable by component substitution) |
| Output Compliance | Up to 10V |
| Allowed Load Resistance | Any resistance ≤ 500Ω |
| Offset and Scale Errors | ±0.04 mA offset error, ±0.05 mA/V compliance error, and ±1% typ gain error added to DAC offset and gain errors. |

# Signal Conditioning Wildcard Hardware

The Signal Conditioning Wildcard contains circuitry that converts the digital to analog (DAC) outputs and analog to digital (ADC) inputs on the Analog I/O Wildcard Field Header to the voltage and current ranges on the Signal Conditioning Wildcard's Field Header as described by the following table:

| Analog I/O Wildcard Field Header | | | | | Signal Conditioning Wildcard Field Header | | |
|---|---|---|---|---|---|---|---|
| Signal | Pins | Range | Channels | | Signal | Pins | Range |
| 12-bit DAC Voltage Output | 24 - 21 | 0 - 4.096 V | DAC0-3 | ↔ | Current Output | 24 - 21 | 0 - 20.48 mA |
| 12-bit DAC Voltage Output | 20 - 17 | 0 - 4.096 V | DAC4-7 | ↔ | Voltage Output | 20 - 17 | 0 - 10.24 V |
| 16-bit ADC Voltage Input | 14 - 11 | 0 - 2.048 V | ADC0-3 | ↔ | Current Input | 14 - 11 | 0 - 20.48 mA |
| 16-bit ADC Voltage Input | 10 - 7 | 0 - 2.048 V | ADC4-7 | ↔ | Voltage Input | 10 - 7 | 0 - 10.24 V |

The Wildcard provides three headers: a Wildcard bus header, a header to connect to the Analog I/O Wildcard's field header, and an Input/Output field header. There is a one-to-one correspondence between the pins on the Analog I/O Wildcard Field Header and the Signal Conditioning Wildcard's Input/Output Field Header. Each I/O signal of the Analog I/O Wildcard is modified by the Signal Conditioning Wildcard (by conversion to/from a greater voltage or current) and presented at the same pin location on its own Input/Output header. The positions of the headers are shown in Figure 1.

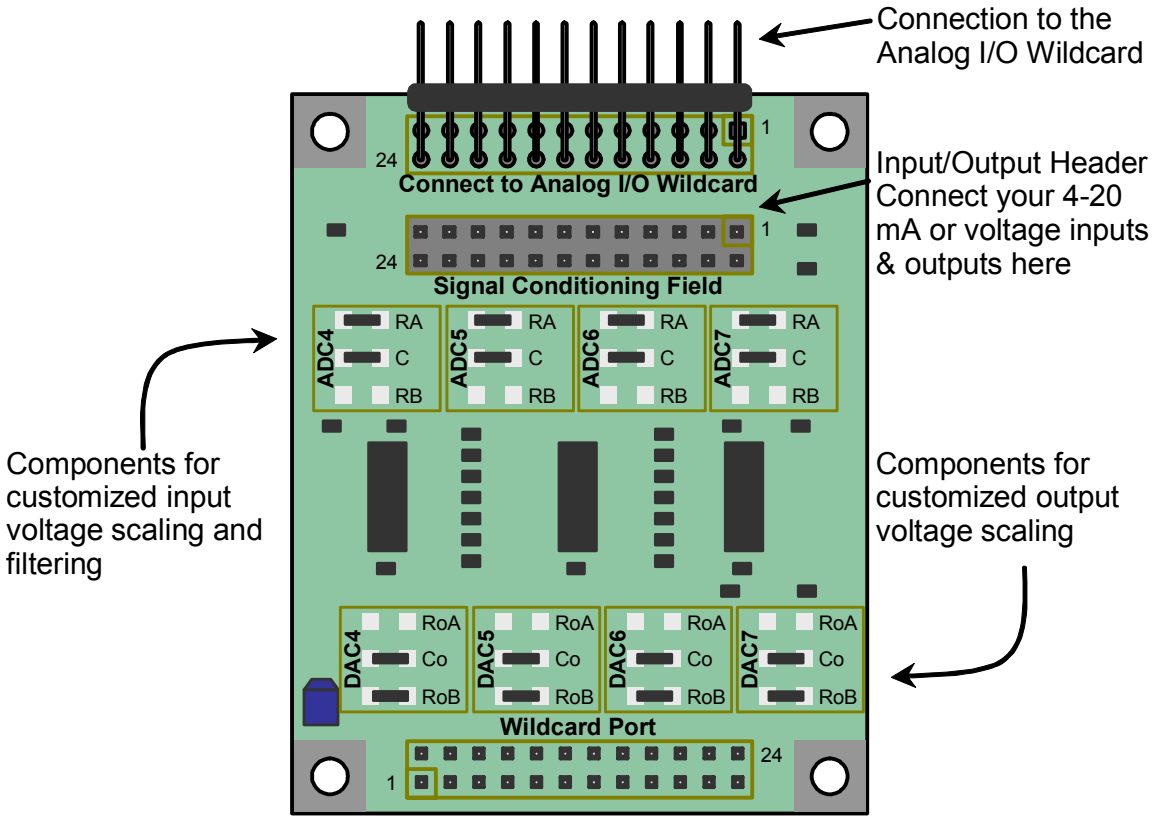



**Figure 1 Signal Conditioning Wildcard showing default configuration components**

# Connecting an Analog I/O Wildcard to the Wildcard Bus

To connect an Analog I/O Wildcard (which is required to use the Signal Conditioning Wildcard) to a Wildcard bus on a controller board, follow these simple steps:

With the power off, connect the female 24-pin side of the stacking go-through Wildcard bus header on the bottom of the Analog I/O Wildcard to Wildcard Port 0 or Wildcard Port 1 on the Wildcard bus on the controller board. The corner mounting holes on the Wildcard should line up with the standoffs on the controller board. The Wildcard ports are labeled on the silkscreen of the controller board. Note that the Analog I/O Wildcard headers are configured to allow direct stacking onto the Wildcard bus, even if other Wildcards are also installed. Do not use ribbon cables to connect the Analog I/O Wildcard to the Wildcard bus.

CAUTION: The Wildcard bus does not have keyed connectors. Be sure to insert the module so that all pins are connected. The Wildcard bus and the Analog I/O Wildcard can be permanently damaged if the connection is done incorrectly. Always make the connection with the power off.

# Configuring the Analog I/O Wildcard

Once you have connected the Analog I/O Wildcard to the Wildcard bus, you must set the address of the module using jumper shunts across J1 and J2.

The Wildcard Select Jumpers, labeled J1 and J2, select a 2-bit code that sets a unique address on the Wildcard port of the Mosaic controller. Each Wildcard port on the Mosaic controller accommodates up to 4 Wildcards. Wildcard Port 0 provides access to modules 0-3 while Wildcard Port 1 provides access to modules 4-7. Two Wildcards on the same port cannot have the same address (jumper settings). The following table shows the possible jumper settings and the corresponding addresses.

| Wildcard Port | ANALOG I/O Wildcard Address | Analog I/O Installed Jumper Shunts |
|---|---|---|
| 0 | 0 | None |
| | 1 | J1 |
| | 2 | J2 |
| | 3 | J1 and J2 |
| 1 | 4 | None |
| | 5 | J1 |
| | 6 | J2 |
| | 7 | J1 and J2 |

Note: On QScreen and Handheld products, Wildcard address 0 is dedicated to their display controller and so is unavailable for mounting Wildcards.

You also need to install J3, which connects the DAC reference pin to the A/D reference input pin, and J6 which connects the reference voltage to pin 4 of the Analog I/O Wildcard field header. No other voltage reference jumpers should be installed. In software, you must set the DAC's internally generated reference voltage to 2.048 volts by passing the constant INT_2V_DAC12 to the Init_Analog_IO function. This will configure the Analog I/O Wildcard's 12-bit DAC output to have a range of 0 to 4.096 volts and its 16-bit A/D input range of 0 to 2.048 volts. Please consult the Analog I/O Wildcard manual for more information.

# Connecting to the Signal Conditioning Wildcard

Once the Analog I/O Wildcard is installed and configured, you can now install the Signal Conditioning Wildcard.

1. With the power off, connect the female 24-pin side of the stacking go-through Wildcard bus header on the bottom of the Signal Conditioning Wildcard on top of your Analog I/O Wildcard. The corner mounting holes on the module should line up with the standoffs on the controller board. Do not use ribbon cables to connect the Signal Conditioning Wildcard to your Analog I/O Wildcard.

2. Connect one end of the 24 pin ribbon cable (shipped with your Signal Conditioning Wildcard) into the Field Header H3 of an Analog I/O Wildcard. Be sure to align the red stripe on the cable to pin one of the header.

3. Connect the other end of the cable into the Analog I/O Field Header, H2 of the Signal Conditioning Wildcard.

Note that using a single 24-pin ribbon cable connects all of the Analog I/O Wildcards inputs and outputs to the Signal Conditioning Wildcard. However, in some applications you may prefer to use some of the Analog I/O signals directly, without filtering through the Signal Conditioning Wildcard. For example, you may not need the 0-20 mA current inputs and outputs of the Signal Conditioning Wildcard. In that case you can still continue to use the Analog I/O Wildcard inputs and outputs that would otherwise be directed to the Signal Conditioning Wildcard by breaking apart the 24-pin cable and making separate connections directly to the Analog I/O Wildcard as needed.

Now you are ready to connect your signals to field header H1 of the Signal Conditioning Wildcard.

# Connecting Power and Grounds

The Wildcard derives its power from the V+RAW and GND pins of the Wildcard bus. This Wildcard requires a somewhat higher voltage supply than most other Wildcards – for proper operation, the V+RAW supply must be in the range of 12.5 to 26 V.

To prevent the creation of ground loops that will induce offset errors into your circuits, be sure to reference all inputs (0 to 20 mA or 0 to 10V) and outputs (0 to 20mA and 0 to 10V) to the ground of pins 5, 6, 15, and 16 on the Input/Output Connector (i.e., not to the digital ground).

# Headers on the Signal Conditioning Wildcard

### *H1 – Input/Output or Field Connector*

The Field connector is a 24-pin header that you use to connect to your external analog signals.

### *H2 – Analog I/O Field Connector*

The Analog I/O Field connector is a 24-pin header that you cable to an Analog I/O Wildcard Field header. A 24-pin cable is provided with the Signal Conditioning Wildcard for this purpose. There may be applications for which you do not wish all of the analog inputs/outputs to pass through the Signal Conditioning Wildcard. In that case you can cable only the signals you wish to use, and run other signals directly in/out of the Analog I/O Wildcard as needed.

### *H3 – Wildcard Bus Connector*

The Wildcard Bus connector is a 24-pin stacking/go through header/socket that allows the Signal Conditioning Wildcard to stack on an Analog I/O Wildcard. Although the Signal Conditioning Wildcard takes its power from this connector, it does not occupy a Wildcard address. Consequently you may use the Signal Conditioning Wildcard without decreasing the number of other Wildcards allowed.

The following table describes the signals on each connector:

**Table 1-1 Signal Conditioning Wildcard Headers**

| H1 Input/Output Header | | | H2 Analog I/O Field | | | H3 Wildcard Bus | | |
|---|---|---|---|---|---|---|---|---|
| **Signal** | **Pins** | **Signal** | **Signal** | **Pins** | **Signal** | **Signal** | **Pins** | **Signal** |
| DIGGND – 1 | 2 – | +5V | GND – 1 | 2 – | +5V | GND – 1 | 2 – | +5V |
| +5VAN – 3 | 4 – | VREF | +5VAN – 3 | 4 – | VREF | /IRQ – 3 | 4 – | V+RAW |
| GND – 5 | 6 – | GND | ADCGND – 5 | 6 – | ADCGND | PG1 – 5 | 6 – | PG0 |
| Vin7 – 7 | 8 – | Vin6 | ADC7 – 7 | 8 – | ADC6 | MOSI – 7 | 8 – | MISO |
| Vin5 – 9 | 10 – | Vin4 | ADC5 – 9 | 10 – | ADC4 | /RESET – 9 | 10 – | SCK |
| Iin3 – 11 | 12 – | Iin2 | ADC3 – 11 | 12 – | ADC2 | /MOD.CS – 11 | 12 – | 16 MHz |
| Iin1 – 13 | 14 – | Iin0 | ADC1 – 13 | 14 – | ADC0 | E – 13 | 14 – | R/W |
| GND – 15 | 16 – | GND | DACGND – 15 | 16 – | DACGND | /OE – 15 | 16 – | /WE |
| Vout7 – 17 | 18 – | Vout6 | DAC7 – 17 | 18 – | DAC6 | AD7 – 17 | 18 – | AD6 |
| Vout5 – 19 | 20 – | Vout4 | DAC5 – 19 | 20 – | DAC4 | AD5 – 19 | 20 – | AD4 |
| Iout3 – 21 | 22 – | Iout2 | DAC3 – 21 | 22 – | DAC2 | AD3 – 21 | 22 – | AD2 |
| Iout1 – 23 | 24 – | Iout0 | DAC1 – 23 | 24 – | DAC0 | AD1 – 23 | 24 – | AD0 |

# Customizing for Different Full-Scale Voltage Ranges

The Signal Conditioning Wildcard has default full scale ranges of 0-20 mA in and out and 0-10V in and out. You can modify these by soldering different components onto the board. Figure 1 shows locations on the board for these components, and it shows which components are installed by default. The following discussion explains which components to change, and how to compute their values, for any full-scale voltage or current range you need.

### *Changing the Input Voltage Range*

In its default configuration the Wildcard accommodates 0–10V full scale input signals. The input voltage is attenuated by a factor of five and filtered by a resistor divider network and presented to a buffer amplifier. The buffer then feeds the resulting 0–2V FS signal to the Analog I/O Wildcard's A/D converter. You can change the attenuation factor or introduce a gain by changing resistors on the board, and you can change the frequency response by changing a capacitor. A simplified schematic of the circuit is shown in Figure 2.

The DC gain of the circuit is given by,

$$G = \frac{V_{out}}{V_{in}} = \frac{R_A}{300 + R_A}\left[\,1 + \frac{75}{R_B}\,\right]$$

where the resistances are in kΩ. The default configuration is not to install $R_B$ and to install 75 kΩ for $R_A$, giving a gain (attenuation) of 0.2. You can change the gain by installing other values.

### *Attenuating Greater Input Voltages*

For example, to operate the circuit as an attenuator for input full scale voltages of any voltage greater than 2.048V you would not install $R_B$, and for $R_A$ install a value given by (in kΩ),

$$R_A = \frac{300 \cdot 2.048}{V_{FS} - 2.048}$$

For a full scale voltage of 10.24 V this gives the default resistance of 75 kΩ. For a full scale voltage of 100V you would use a resistance of 6.2 kΩ.

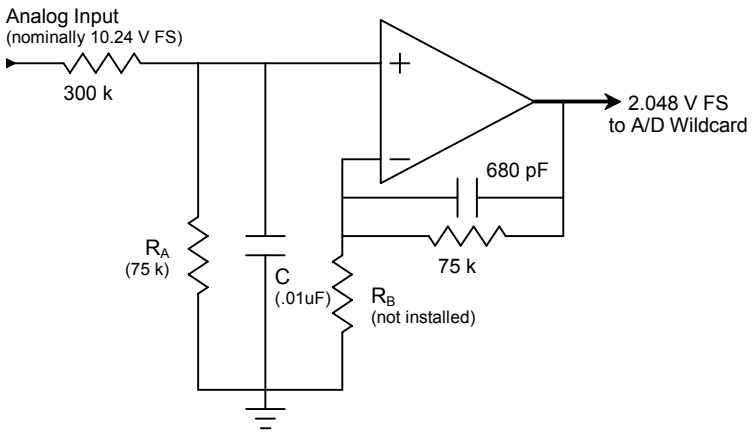



**Figure 2** **The input buffer is programmable for attenuation or amplification. The values installed for a default full-scale input of 10.24 V are shown in parentheses.**

### *Amplifying Small Input Voltages*

To amplify signals whose full scale is less than 2.048V, you would not install $R_A$ and instead install a value of $R_B$ given by (in kΩ),

$$R_B = \frac{75\ V_{FS}}{2.048 - V_{FS}}$$

For example, for a full scale input voltage of 0.1V, $R_B$=3.85 kΩ.

### *Offset and Gain Errors*

In attenuation mode, the op-amp's offset error appears as a ±2mV offset on the 2.048V FS signal sent to the A/D. In amplification mode, the op-amp's offset error is also amplified and is increased to ±2mV*2.048/$V_{inFS}$. Full scale gain errors result from imprecision in resistor values; when using 1% resistors the full scale gain error is ±1-2%.

### *Adjusting the Anti-Aliasing Low-Pass Filter Cut-Off Frequency*

Owing to the capacitors in the input network and in the feedback loop, the circuit acts as an anti-aliasing filter with two low-pass cutoff frequencies. When the circuit amplifies, the feedback loop capacitor causes the gain to drop off with a 3dB cut-off frequency of 3.1 kHz, dropping eventually to unity gain. In either attenuation or gain mode there is an additional low-pass cut-off frequency given by,

$$fc = \frac{300 + R_A}{600\ \pi\ R_A C}$$

where the frequency is given in kHz for $R_A$ in kΩ and C in microfarads. In the default configuration $R_A$ = 75 kΩ, C=0.01 μF, and the cut-off frequency is 265 Hz. You can change the cutoff frequency by installing an appropriate value of capacitance.

## *Changing the Output Voltage Range*

In its default configuration, the Wildcard outputs four 0–10.24V output signals. This output is created by amplifying a 0–4.096 voltage range from the Analog I/O Wildcard's DACs, and buffering it. You can change the gain factor, or attenuate, by changing resistors on the board, and you can change the frequency response of the output by changing a capacitor. A simplified schematic of the circuit is shown in Figure 3:

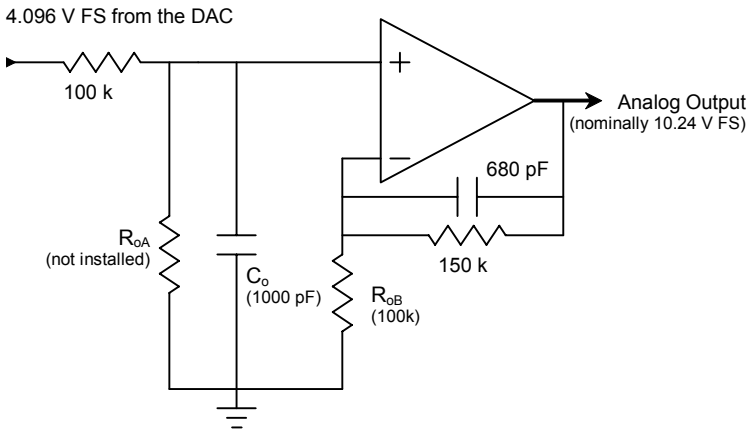



**Figure 3 The output buffer is programmable for attenuation or amplification. The values installed for a default full-scale output of 10.24V are shown in parentheses.**

The DC gain of the circuit is given by,

$$G = \frac{V_{out}}{V_{in}} = \frac{R_{oA}}{100 + R_{oA}} \left[ 1 + \frac{150}{R_{oB}} \right]$$

where the resistances are in kΩ. The default configuration is to not install $R_{oA}$ and to install 100 kΩ for $R_{oB}$, giving a gain of 2.5 so that the full scale output is 10.24V. You can change the gain by installing other values.

## *Producing Output Voltages Greater than 4 V Full Scale*

For example, to produce any full scale output voltage greater than 4.096V you would not install $R_{OA}$, and for $R_{oB}$ install a value given by (in kΩ),

$$R_{oB} = \frac{150 \cdot 4.096}{V_{FS} - 4.096}$$

For a full scale voltage of 10.24 V this gives the default resistance of 100 kΩ. For a full scale voltage of 5.12V you would use a resistance of 600 kΩ.

### *Producing Output Voltages Less than 4 V Full Scale*

To produce smaller output voltages, with the full scale output less than 4.096V, you would not install $R_{oB}$ and install a value of $R_{oA}$ given by (in kΩ),

$$R_{oA} = \frac{100\ V_{FS}}{4.096 - V_{FS}}$$

For example, for a full scale output voltage of 1.024V, $R_{oA}$=33.3 kΩ.

### *Offset and Gain Errors*

In attenuation mode, the op-amp's offset error appears as a ±2mV offset on the full scale output voltage. In amplification mode, the op-amp's offset error is also amplified and is increased to ±2mV* $V_{outFS}$ /4.096. Full scale gain errors result from imprecision in resistor values, and using 1% resistors the full scale gain error is ±1-2%.

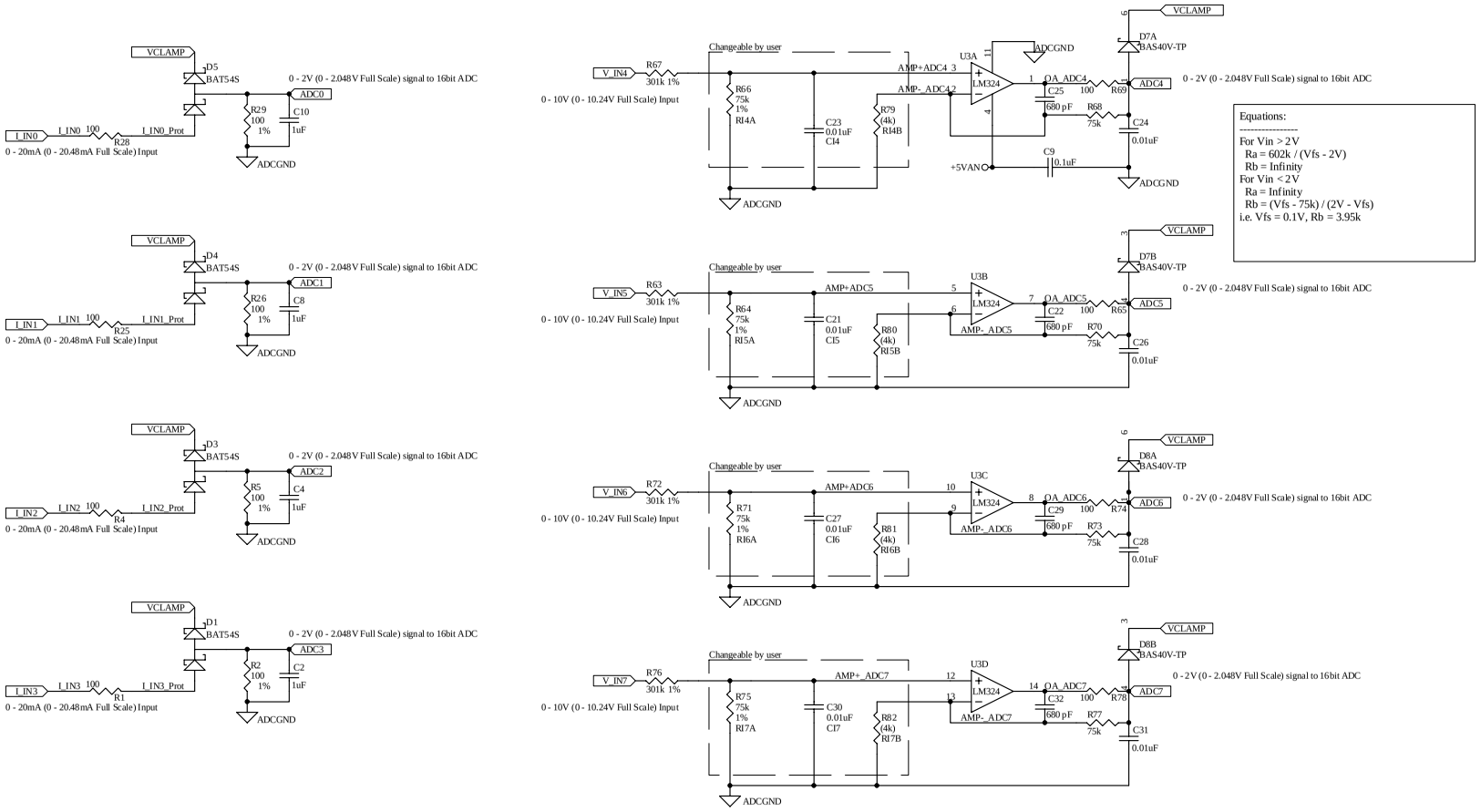
### *Adjusting the Output Low-Pass Filter Cut-Off Frequency*

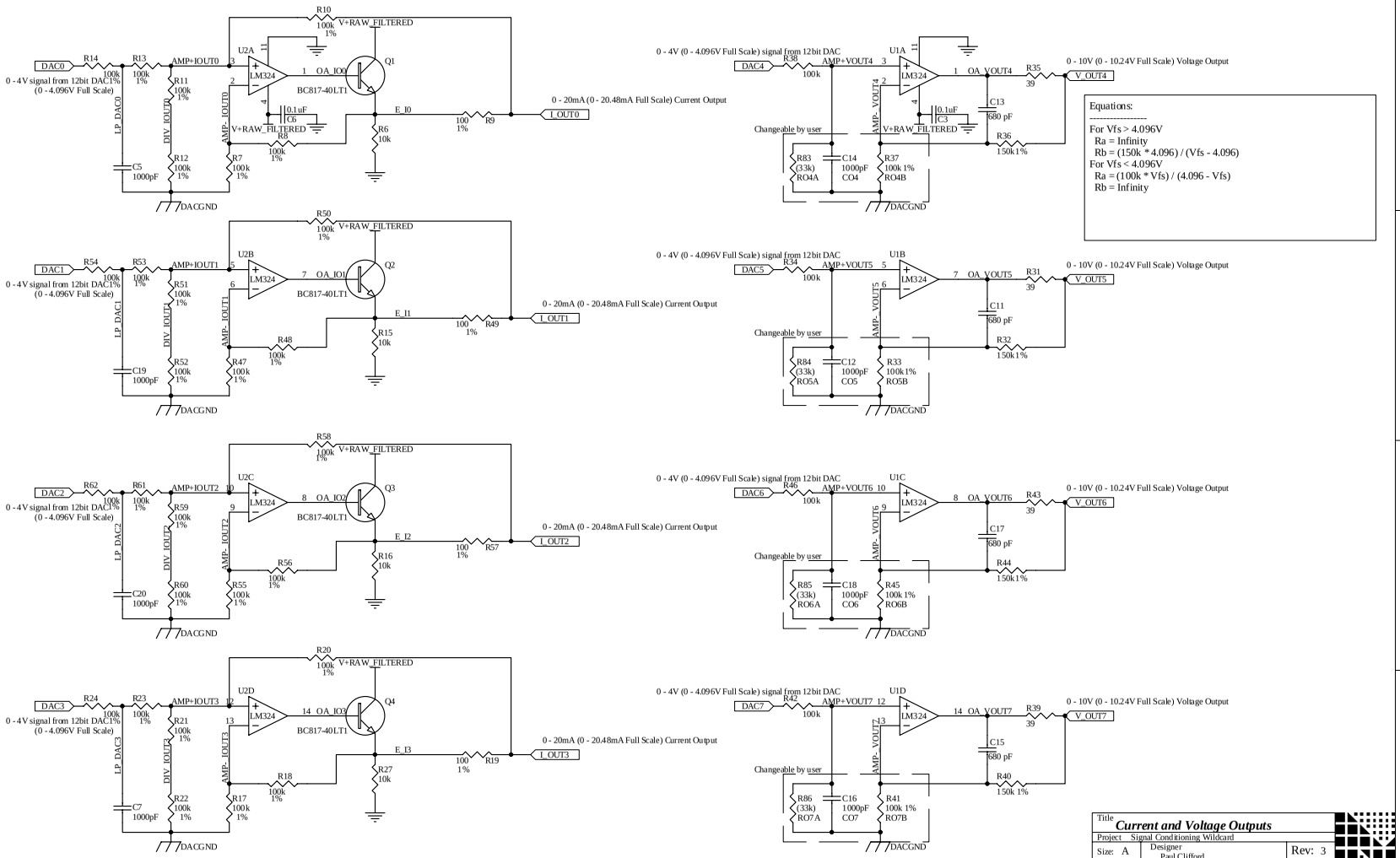
You can lessen the high frequency content of the output when a step is made, thereby softening the step, by increasing the output filter capacitance. Two capacitors in the buffer produce a two-pole low-pass filter. When the circuit amplifies, the feedback loop capacitor causes the gain to drop off with a 3dB cut-off frequency of 1.6 kHz, dropping eventually to unity gain. In either attenuation or gain mode there is an additional low-pass cut-off frequency given by,

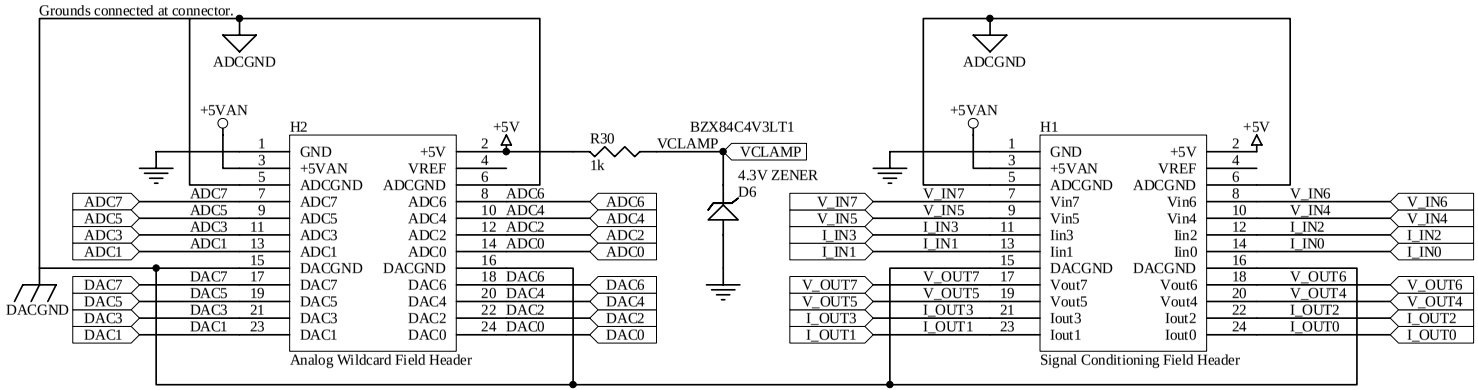
$$fc = \frac{100 + R_{oA}}{200\ \pi\ R_{oA} C_o}$$

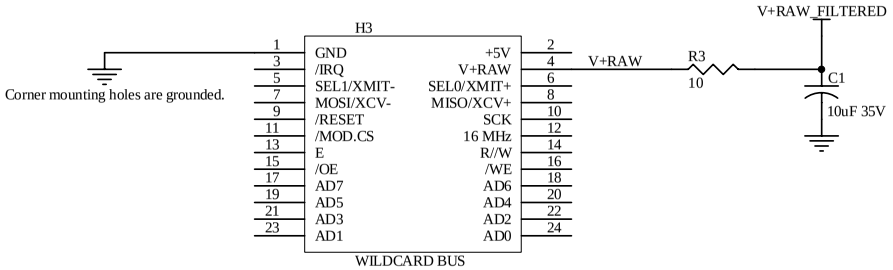
where the frequency is given in kHz for $R_{oA}$ in kΩ and C in microfarads. In the default configuration $R_{oA}$ is not installed (we take the limit of the above equation as $R_{oA}$ goes to infinity), $C_o$=0.001 μF, and the cut-off frequency is 1.6 kHz. You can lower the cutoff frequency further by installing a greater value of capacitance.

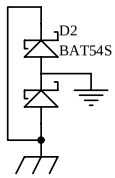
# Detailed Hardware Schematics


VCLAMP
D5
BAT54S
0 - 2V (0 - 2.048V Full Scale) signal to 16bit ADC
ADC0
R29
100
1%
C10
1uF
I_IN0
I_IN0
100
R28
I_IN0_Prot
0 - 20mA (0 - 20.48mA Full Scale) Input
ADCGND
VCLAMP
D4
BAT54S
0 - 2V (0 - 2.048V Full Scale) signal to 16bit ADC
ADC1
R26
100
1%
C8
1uF
I_IN1
I_IN1
100
R25
I_IN1_Prot
0 - 20mA (0 - 20.48mA Full Scale) Input
ADCGND
VCLAMP
D3
BAT54S
0 - 2V (0 - 2.048V Full Scale) signal to 16bit ADC
ADC2
R5
100
1%
C4
1uF
I_IN2
I_IN2
100
R4
I_IN2_Prot
0 - 20mA (0 - 20.48mA Full Scale) Input
ADCGND
VCLAMP
D1
BAT54S
0 - 2V (0 - 2.048V Full Scale) signal to 16bit ADC
ADC3
R2
100
1%
C2
1uF
I_IN3
I_IN3
100
R1
I_IN3_Prot
0 - 20mA (0 - 20.48mA Full Scale) Input
ADCGND
Changeable by user
V_IN4
R67
301k 1%
0 - 10V (0 - 10.24V Full Scale) Input
R66
75k
1%
RI4A
C23
0.01uF
CI4
R79
(4k)
RI4B
AMP+ADC4
AMP-_ADC4
U3A
LM324
ADCGND
OA_ADC4
C25
680 pF
R68
75k
R69
100
ADC4
C24
0.01uF
0 - 2V (0 - 2.048V Full Scale) signal to 16bit ADC
C9
0.1uF
+5VANO
ADCGND
VCLAMP
D7A
BAS40V-TP
Equations:
For Vin > 2V
Ra = 602k / (Vfs - 2V)
Rb = Infinity
For Vin < 2V
Ra = Infinity
Rb = (Vfs - 75k) / (2V - Vfs)
i.e. Vfs = 0.1V, Rb = 3.95k
Changeable by user
V_IN5
R63
301k 1%
0 - 10V (0 - 10.24V Full Scale) Input
R64
75k
1%
RI5A
C21
0.01uF
CI5
R80
(4k)
RI5B
AMP+ADC5
AMP-_ADC5
U3B
LM324
ADCGND
OA_ADC5
C22
680 pF
R70
75k
R65
100
ADC5
C26
0.01uF
0 - 2V (0 - 2.048V Full Scale) signal to 16bit ADC
VCLAMP
D7B
BAS40V-TP
Changeable by user
V_IN6
R72
301k 1%
0 - 10V (0 - 10.24V Full Scale) Input
R71
75k
1%
RI6A
C27
0.01uF
CI6
R81
(4k)
RI6B
AMP+ADC6
AMP-_ADC6
U3C
LM324
ADCGND
OA_ADC6
C29
680 pF
R73
75k
R74
100
ADC6
C28
0.01uF
0 - 2V (0 - 2.048V Full Scale) signal to 16bit ADC
VCLAMP
D8A
BAS40V-TP
Changeable by user
V_IN7
R76
301k 1%
0 - 10V (0 - 10.24V Full Scale) Input
R75
75k
1%
RI7A
C30
0.01uF
CI7
R82
(4k)
RI7B
AMP+_ADC7
AMP-_ADC7
U3D
LM324
ADCGND
OA_ADC7
C32
680 pF
R77
75k
R78
100
ADC7
C31
0.01uF
0 - 2V (0 - 2.048V Full Scale) signal to 16bit ADC
VCLAMP
D8B
BAS40V-TP
Title
Current and Voltage Inputs
Project Signal Conditioning Wildcard
Size: A
Designer
Paul Clifford
Rev: 3
File: IV_Inputs.Sch
Sheet 1 of 3
Date: 4-Jan-2007
11:30:26
Mosaic Industries


R10
100k
1%
V+RAW_FILTERED
DAC0
R14
100k
1%
R13
100k
1%
AMP+IOUT0
0 - 4V signal from 12bit DAC.
(0 - 4.096V Full Scale)
U2A
LM324
OA_IO0
Q1
BC817-40LT1
E_I0
R9
100
1%
I_OUT0
0 - 20mA (0 - 20.48mA Full Scale) Current Output
R11
100k
1%
R12
100k
1%
C5
1000pF
LP_DAC0
DIV_IOUT0
AMP-_IOUT0
0.1uF
C6
R8
100k
1%
R6
10k
R7
100k
1%
DACGND
0 - 4V (0 - 4.096V Full Scale) signal from 12bit DAC
DAC4
R38
100k
AMP+VOUT4
U1A
LM324
OA_VOUT4
R35
39
V_OUT4
0 - 10V (0 - 10.24V Full Scale) Voltage Output
AMP-_VOUT4
C13
680 pF
C3
0.1uF
V+RAW_FILTERED
R36
150k
1%
Changeable by user
R83
(33k)
RO4A
C14
1000pF
CO4
R37
100k
1%
RO4B
DACGND
Equations:
For Vfs > 4.096V
Ra = Infinity
Rb = (150k * 4.096) / (Vfs - 4.096)
For Vfs < 4.096V
Ra = (100k * Vfs) / (4.096 - Vfs)
Rb = Infinity
R50
100k
1%
V+RAW_FILTERED
DAC1
R54
100k
1%
R53
100k
1%
AMP+IOUT1
0 - 4V signal from 12bit DAC.
(0 - 4.096V Full Scale)
U2B
LM324
OA_IO1
Q2
BC817-40LT1
E_I1
R49
100
1%
I_OUT1
0 - 20mA (0 - 20.48mA Full Scale) Current Output
R51
100k
1%
R52
100k
1%
C19
1000pF
LP_DAC1
DIV_IOUT1
AMP-_IOUT1
R48
100k
1%
R15
10k
R47
100k
1%
DACGND
0 - 4V (0 - 4.096V Full Scale) signal from 12bit DAC
DAC5
R34
100k
AMP+VOUT5
U1B
LM324
OA_VOUT5
R31
39
V_OUT5
0 - 10V (0 - 10.24V Full Scale) Voltage Output
AMP-_VOUT5
C11
680 pF
Changeable by user
R84
(33k)
RO5A
C12
1000pF
CO5
R33
100k
1%
RO5B
R32
150k
1%
DACGND
R58
100k
1%
V+RAW_FILTERED
DAC2
R62
100k
1%
R61
100k
1%
AMP+IOUT2
0 - 4V signal from 12bit DAC.
(0 - 4.096V Full Scale)
U2C
LM324
OA_IO2
Q3
BC817-40LT1
E_I2
R57
100
1%
I_OUT2
0 - 20mA (0 - 20.48mA Full Scale) Current Output
R59
100k
1%
R60
100k
1%
C20
1000pF
LP_DAC2
DIV_IOUT2
AMP-_IOUT2
R56
100k
1%
R16
10k
R55
100k
1%
DACGND
0 - 4V (0 - 4.096V Full Scale) signal from 12bit DAC
DAC6
R46
100k
AMP+VOUT6
U1C
LM324
OA_VOUT6
R43
39
V_OUT6
0 - 10V (0 - 10.24V Full Scale) Voltage Output
AMP-_VOUT6
C17
680 pF
Changeable by user
R85
(33k)
RO6A
C18
1000pF
CO6
R45
100k
1%
RO6B
R44
150k
1%
DACGND
R20
100k
1%
V+RAW_FILTERED
DAC3
R24
100k
1%
R23
100k
1%
AMP+IOUT3
0 - 4V signal from 12bit DAC.
(0 - 4.096V Full Scale)
U2D
LM324
OA_IO3
Q4
BC817-40LT1
E_I3
R19
100
1%
I_OUT3
0 - 20mA (0 - 20.48mA Full Scale) Current Output
R21
100k
1%
R22
100k
1%
C7
1000pF
LP_DAC3
DIV_IOUT3
AMP-_IOUT3
R18
100k
1%
R27
10k
R17
100k
1%
DACGND
0 - 4V (0 - 4.096V Full Scale) signal from 12bit DAC
DAC7
R42
100k
AMP+VOUT7
U1D
LM324
OA_VOUT7
R39
39
V_OUT7
0 - 10V (0 - 10.24V Full Scale) Voltage Output
AMP-_VOUT7
C15
680 pF
Changeable by user
R86
(33k)
RO7A
C16
1000pF
CO7
R41
100k
1%
RO7B
R40
150k
1%
DACGND
Title
Current and Voltage Outputs
Project Signal Conditioning Wildcard
Size: A
Designer
Paul Clifford
Rev: 3
File: IV_Outputs.Sch
Sheet 2 of 3
Date: 4-Jan-2007
11:29:35
Mosaic Industries




Diode to prevent grounds from separating too much.

Note:

This Wildcard stacks on the Wildcard bus and connects to the field header of the Analog I/O Wildcard. This Signal Conditioning Wildcard passes four 0-20mA current inputs and four 0-10V voltage inputs to the octal 16-bit A/D on the Analog I/O Wildcard and delivers four 0-20mA current outputs and four 0-10V voltage outputs from the octal 12-bit DAC on the Analog I/O Wildcard.

On the Analog I/O Wildcard, install J3 to connect the DAC reference to the A/D reference input. Thus the 16-bit A/D input range is 0 to 2.048V and the DAC output range is 0 to 4.096V. Also, install J6 to connect the DAC's 2.048 reference voltage to the VREF pin (pin 4) on the Analog I/O Field Header.

For proper operation V+RAW must be greater than 12.5V.

| | | |
|---|---|---|
| Title: ***Headers*** | | |
| Project: Signal Conditioning Wildcard | | |
| Size: A | Designer: Paul Clifford | Rev: 3 |
| File: Headers.Sch | | |
| Sheet 3 of 3 | Date: 15-Dec-2006 12:23:31 | Mosaic Industries |