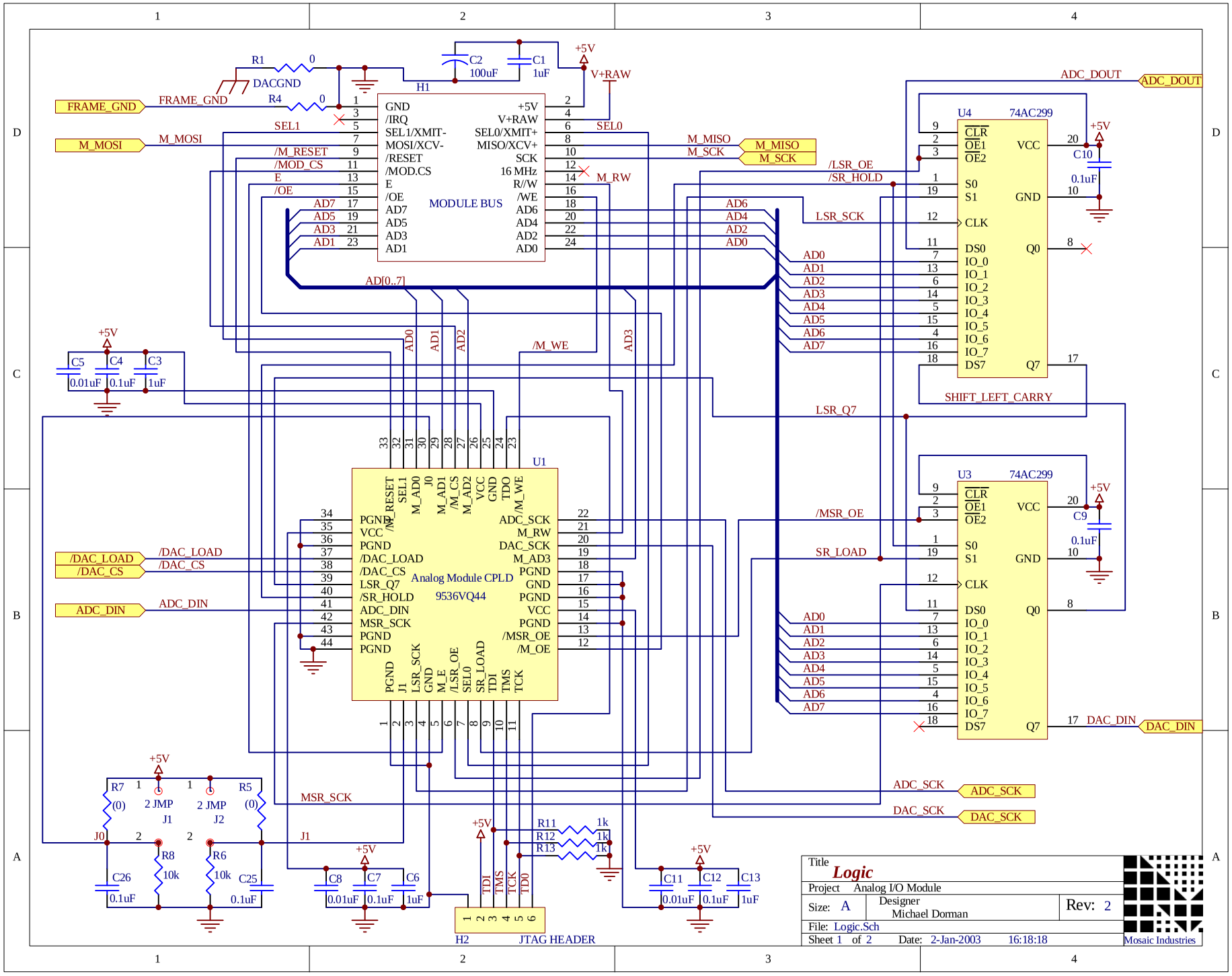
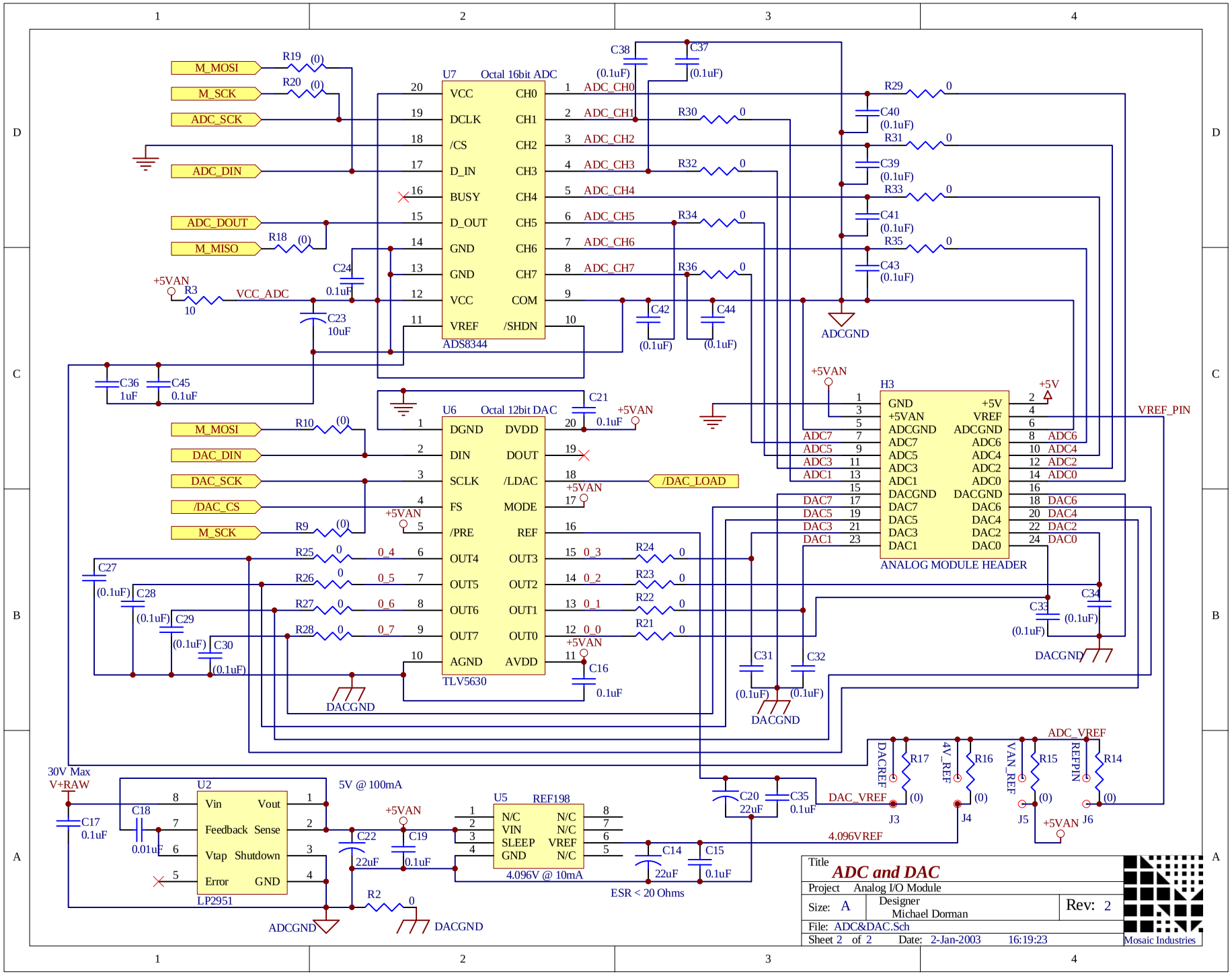

R1 0
DACGND
R4 0
FRAME_GND
FRAME_GND
C2 100uF
C1 1uF
+5V
V+RAW
H1
GND
/IRQ
SEL1/XMIT-
MOSI/XCV-
/RESET
/MOD.CS
E
/OE
AD7
AD5
AD3
AD1
+5V
V+RAW
SEL0/XMIT+
MISO/XCV+
SCK
16 MHz
R//W
/WE
AD6
AD4
AD2
AD0
MODULE BUS
SEL1
SEL0
M_MOSI
M_MISO
M_SCK
/M_RESET
/MOD_CS
E
/OE
M_RW
AD[0..7]
ADC_DOUT
U4 74AC299
U3 74AC299
/LSR_OE
/SR_HOLD
LSR_SCK
LSR_Q7
SHIFT_LEFT_CARRY
/MSR_OE
SR_LOAD
/M_WE
C5 0.01uF
C4 0.1uF
C3 1uF
C10 0.1uF
C9 0.1uF
U1
Analog Module CPLD
9536VQ44
/DAC_LOAD
/DAC_CS
ADC_DIN
DAC_DIN
ADC_SCK
DAC_SCK
MSR_SCK
R7 (0)
R5 (0)
2 JMP J1
2 JMP J2
R8 10k
R6 10k
C26 0.1uF
C25 0.1uF
C8 0.01uF
C7 0.1uF
C6 1uF
R11 1k
R12 1k
R13 1k
C11 0.01uF
C12 0.1uF
C13 1uF
TDI
TMS
TCK
TDO
H2
JTAG HEADER
Title
Logic
Project Analog I/O Module
Size: A
Designer Michael Dorman
Rev: 2
File: Logic.Sch
Sheet 1 of 2
Date: 2-Jan-2003 16:18:18
Mosaic Industries


M_MOSI
M_SCK
ADC_SCK
ADC_DIN
ADC_DOUT
M_MISO
R19 (0)
R20 (0)
R18 (0)
U7 Octal 16bit ADC
VCC CH0 ADC_CH0
DCLK CH1 ADC_CH1
/CS CH2 ADC_CH2
D_IN CH3 ADC_CH3
BUSY CH4 ADC_CH4
D_OUT CH5 ADC_CH5
GND CH6 ADC_CH6
GND CH7 ADC_CH7
VCC COM
VREF /SHDN
ADS8344
C38 (0.1uF)
C37 (0.1uF)
R29 0
R30 0
R31 0
R32 0
R33 0
R34 0
R35 0
R36 0
C40 (0.1uF)
C39 (0.1uF)
C41 (0.1uF)
C43 (0.1uF)
C42 (0.1uF)
C44 (0.1uF)
C24 0.1uF
+5VAN
R3 10
VCC_ADC
C23 10uF
C36 1uF
C45 0.1uF
ADCGND
U6 Octal 12bit DAC
DGND DVDD
DIN DOUT
SCLK /LDAC
FS MODE
/PRE REF
OUT4 OUT3
OUT5 OUT2
OUT6 OUT1
OUT7 OUT0
AGND AVDD
TLV5630
C21 0.1uF
M_MOSI
DAC_DIN
DAC_SCK
/DAC_CS
M_SCK
R10 (0)
R9 (0)
/DAC_LOAD
R25 0
R26 0
R27 0
R28 0
R24 0
R23 0
R22 0
R21 0
C27 (0.1uF)
C28 (0.1uF)
C29 (0.1uF)
C30 (0.1uF)
C16 0.1uF
DACGND
H3
GND +5V
+5VAN VREF
ADCGND ADCGND
ADC7 ADC6
ADC5 ADC4
ADC3 ADC2
ADC1 ADC0
DACGND DACGND
DAC7 DAC6
DAC5 DAC4
DAC3 DAC2
DAC1 DAC0
ANALOG MODULE HEADER
VREF_PIN
C34 (0.1uF)
C33 (0.1uF)
C31 (0.1uF)
C32 (0.1uF)
30V Max
V+RAW
C17 0.1uF
U2
Vin Vout
Feedback Sense
Vtap Shutdown
Error GND
LP2951
C18 0.01uF
5V @ 100mA
C22 22uF
C19 0.1uF
R2 0
U5 REF198
N/C N/C
VIN N/C
SLEEP VREF
GND N/C
4.096V @ 10mA
C14 22uF
C15 0.1uF
ESR < 20 Ohms
C20 22uF
C35 0.1uF
DAC_VREF
4.096VREF
ADC_VREF
DACREF R17
4V_REF R16
VAN_REF R15
REFPIN R14
J3
J4
J5
J6
Title
ADC and DAC
Project Analog I/O Module
Size: A
Designer Michael Dorman
Rev: 2
File: ADC&DAC.Sch
Sheet 2 of 2
Date: 2-Jan-2003 16:19:23
Mosaic Industries